Design and Test
Who sets the direction?

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IMTR Workshop (ETS'25), May 30, 2025

Infineon at a glance

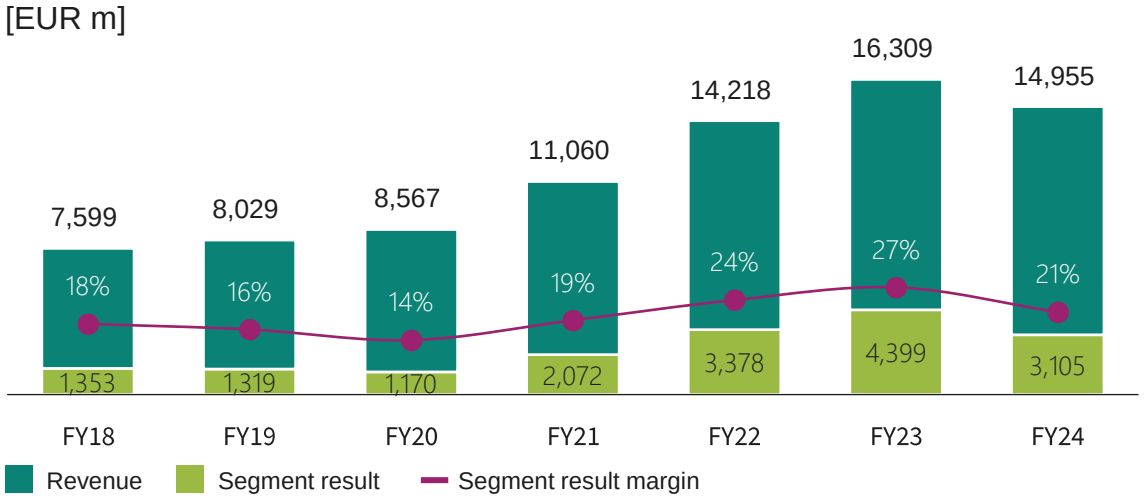
Growth areas

Energy
green and efficient

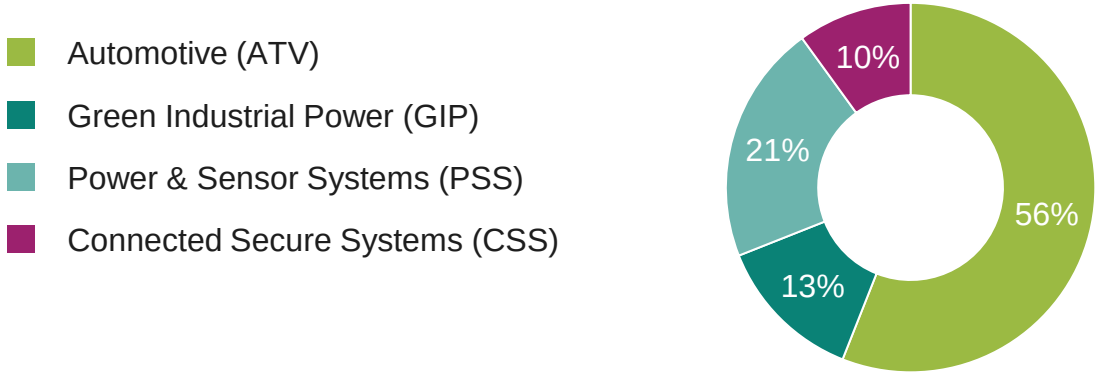
Mobility
clean and safe

IoT
smart and secure

Financials



FY24 revenue by segment[1]

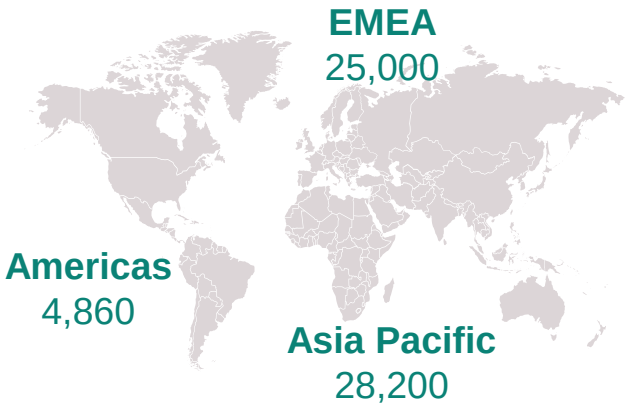


Employees[1]

58,060
employees worldwide

71
R&D and

15
manufacturing locations[2]



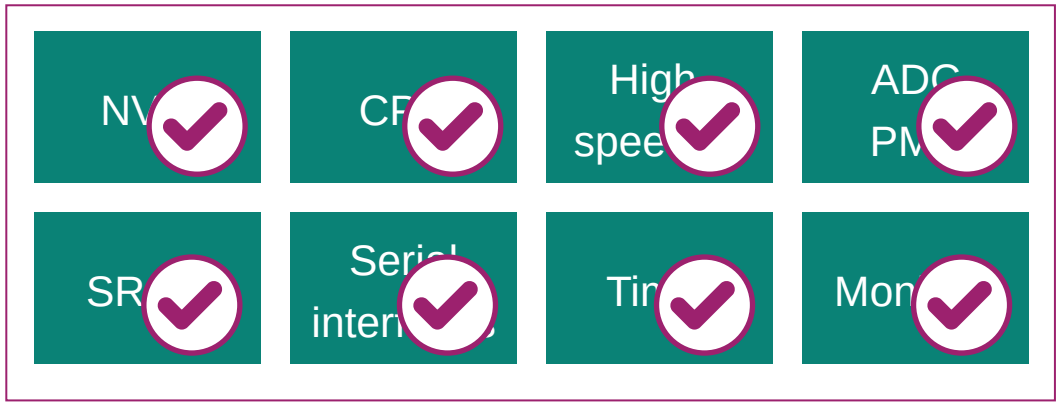
For further information: Infineon Annual Report.
1 2024 Fiscal year (as of 30 September 2024) | **2** As of 30 September 2024

Do you know how deep the water is?

About me

Who sets the direction?

The future needs BIST, BIST, BIST

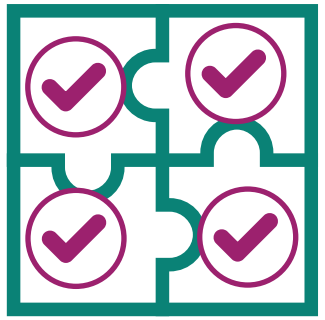


On the way to Chiplets

- Modularity enables scalability and flexibility
- More focused products
- Testability challenges

Autonomous testable units

- Right quality
- Low application time
- Solves access issues
- Agnostic to system functions



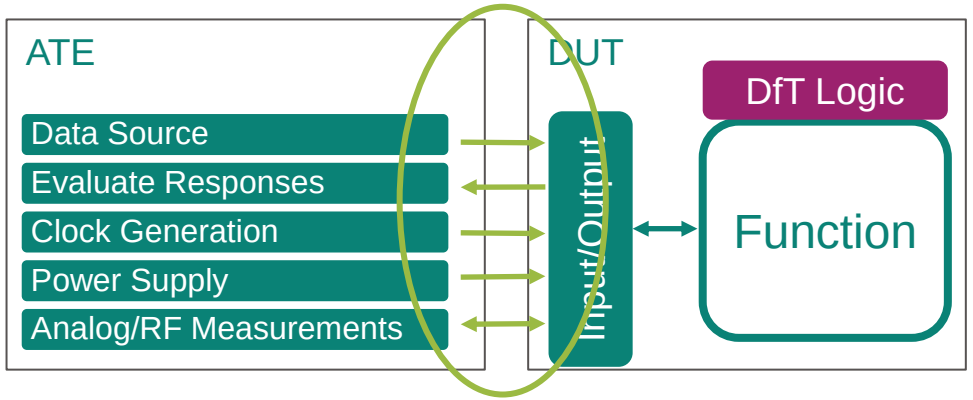
BIST

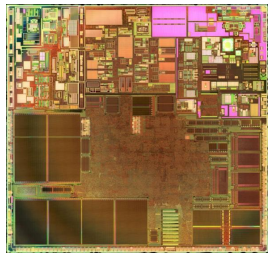
- Enable on-chip concurrency
- Overcome pad performance bottleneck and other access issues
- Reduce demand on pattern memory
- Have more features available in the field

- Controlled timing, voltage, temperature by ATE and test cell
- Shmoos
- Diagnosis for test program stabilization and yield

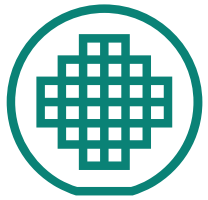
ATE

Design and Test:
There is always a business case to optimize





X s vs. Y mm²



Spend efforts on Silicon (i.e. area)

- (Better) access to internal nodes, modules
- Enable partitioning for test
- Allows on-chip and on-tester parallelism

Design-for-Test uses EDA-driven solutions

- Test control (JTAG or iJTAG)
- Scan and scan compression
- Built-In Self-Test for logic and embedded memories

Design-for-Test serves

- Competitive test cost
- Predictable and reduced product schedules
- Quality, reliability and safety targets

AURIX™ family of automotive microcontrollers

Family of 32-bit microcontrollers

- High performance and low power consumption
- Support for multiple operating systems, including AUTOSAR
- Advanced safety features, such as multiple cores and memory protection units
- Wide range of applications, including automotive and industrial systems

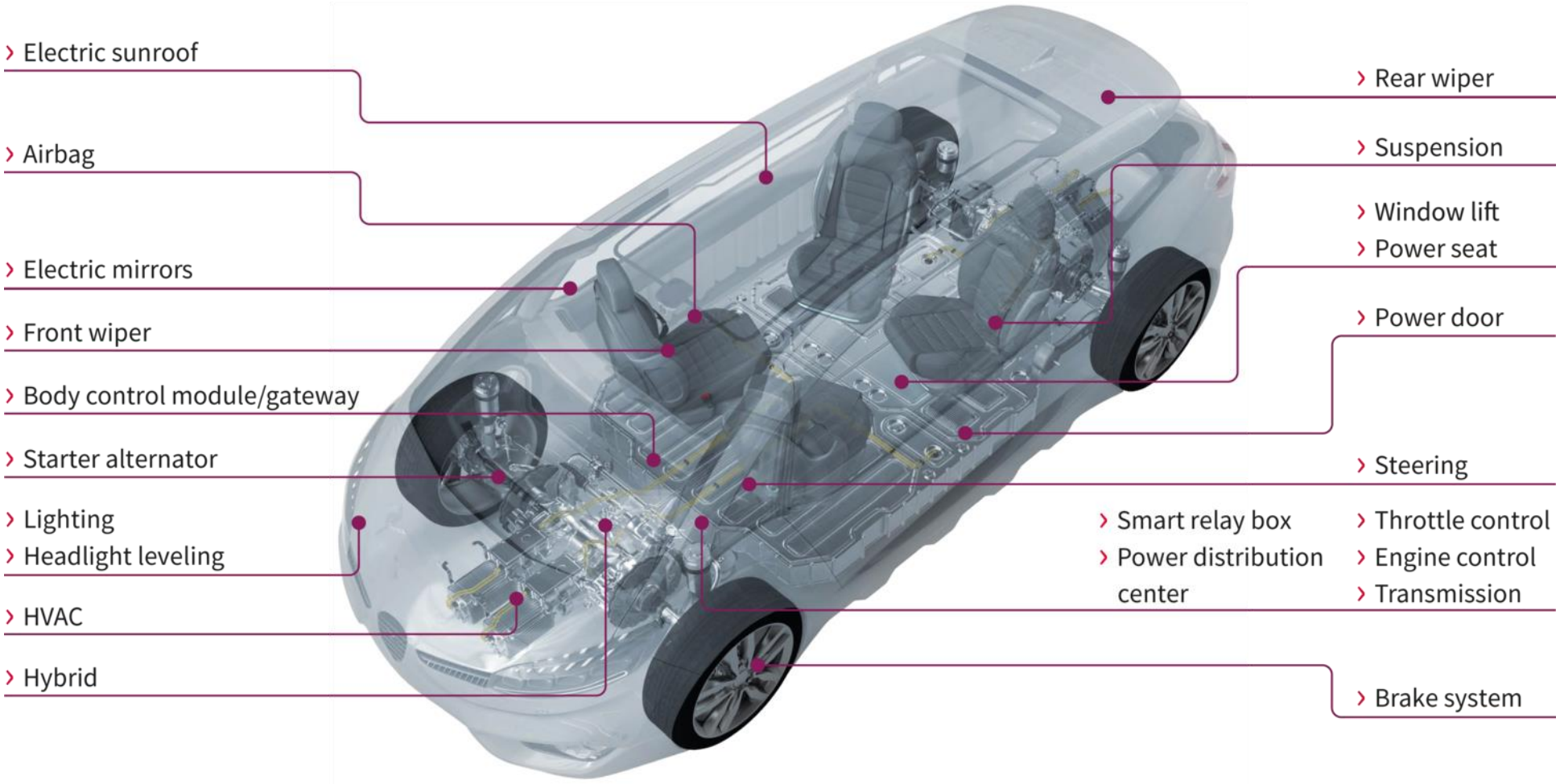
Heterogenous devices

- Embedded Non-Volatile RAM
- Complex Analog like ADC and Power Management
- High-speed PHY interfaces like ETH and PCIe
- Standard logic and SRAM

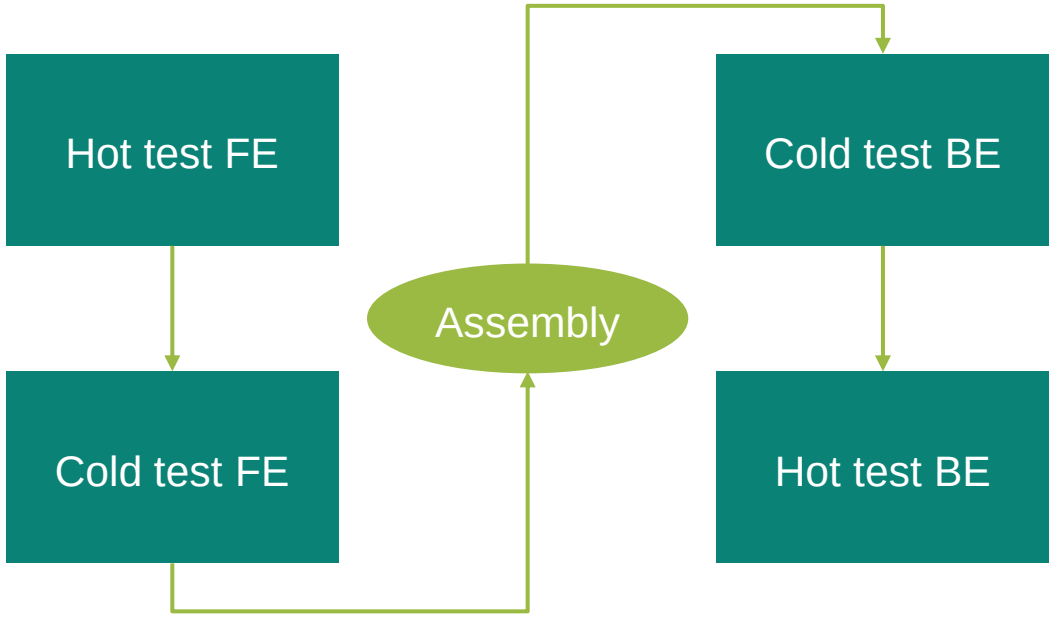
NVM	CPU	High-speed IO	ADC PMS
SRAM	Serial interfaces	Timer	Monitors

MCU family serves automotive applications with different performance and safety requirements

Automotive applications



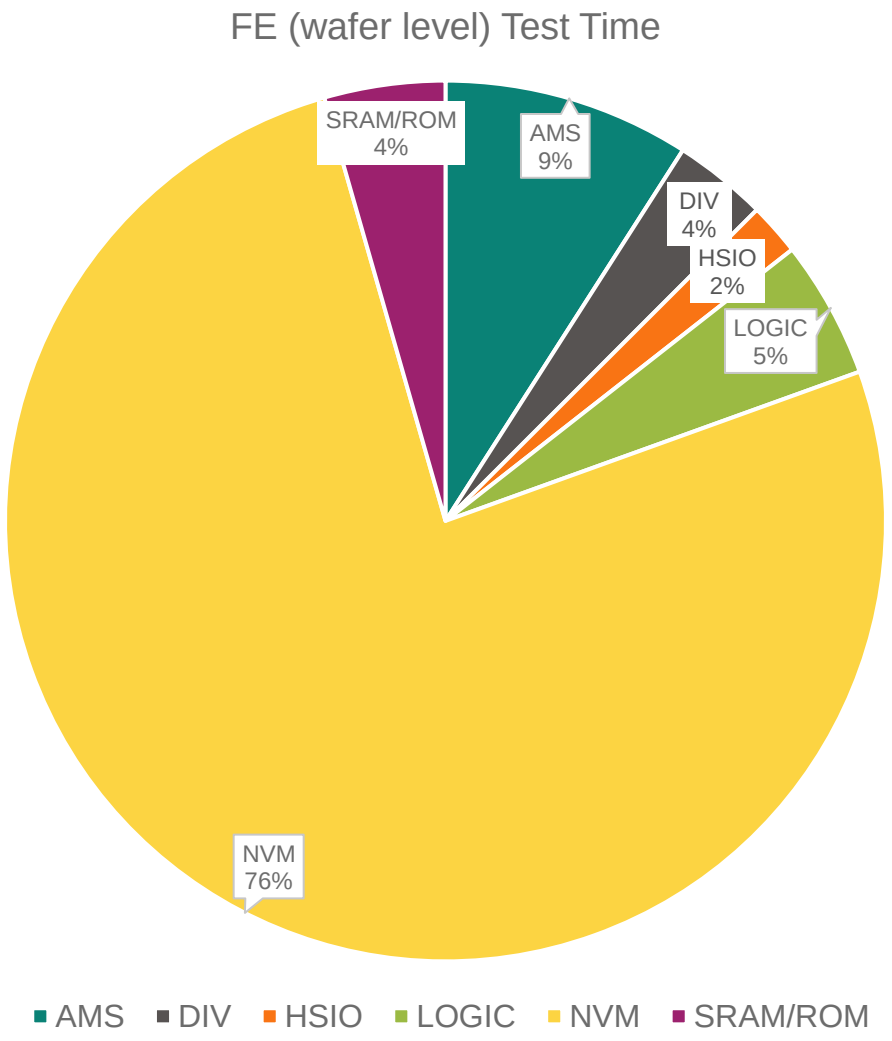
Manufacturing test flow for automotive microcontrollers

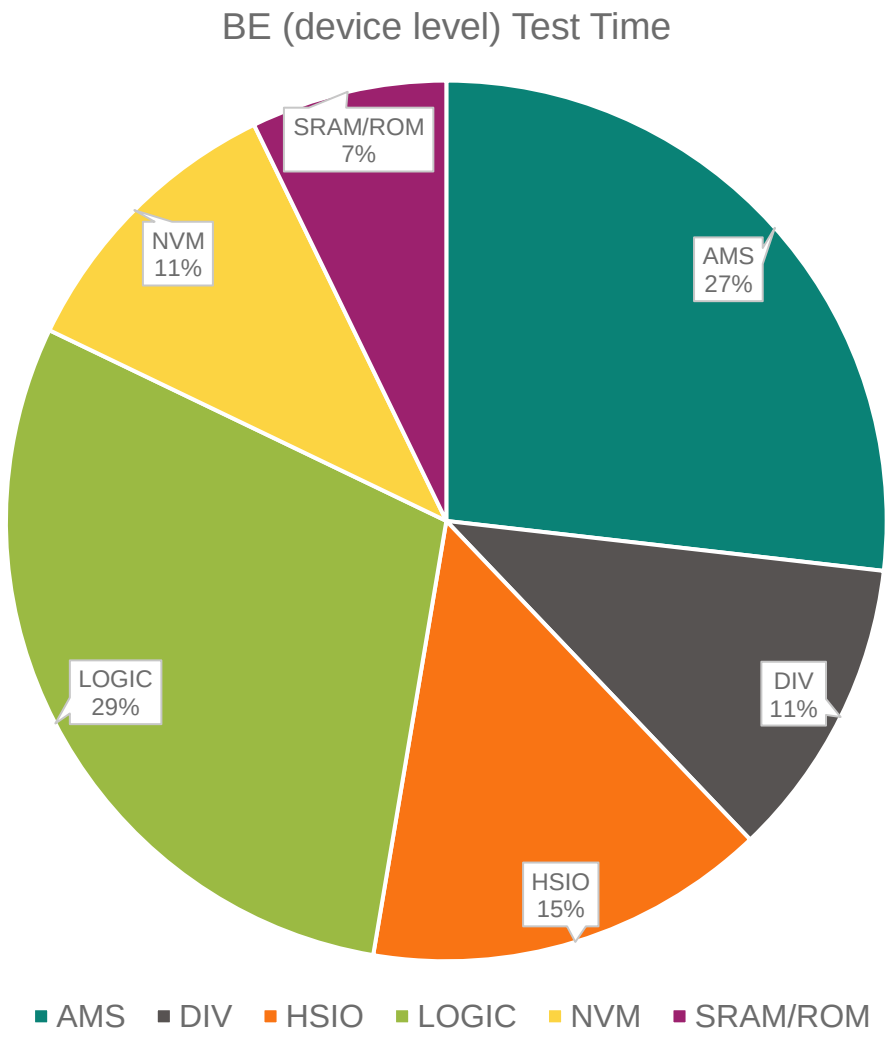


Not shown here

- Bake insertions required for NVM
- Stress test required for automotive
  - Burn-in in BE test
  - High-voltage stress on wafer

Test time distribution for automotive microcontrollers: NVM test is dominating for wafer test

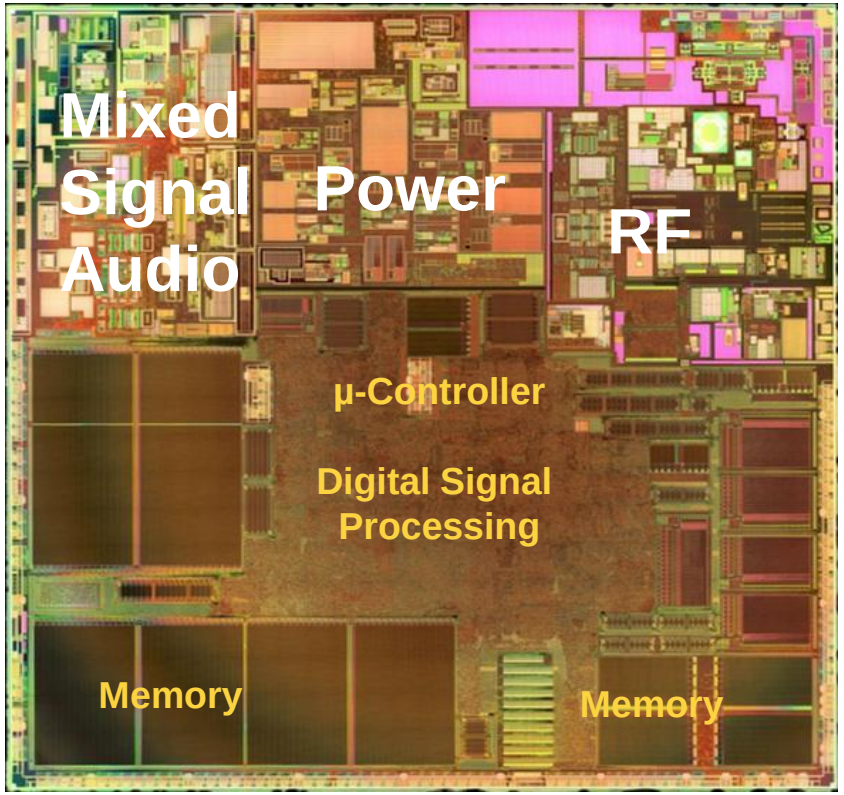




To compare: Test time distribution for a mobile SoC device RF, AMS and PMU dominating

Single chip, low-cost mobile device

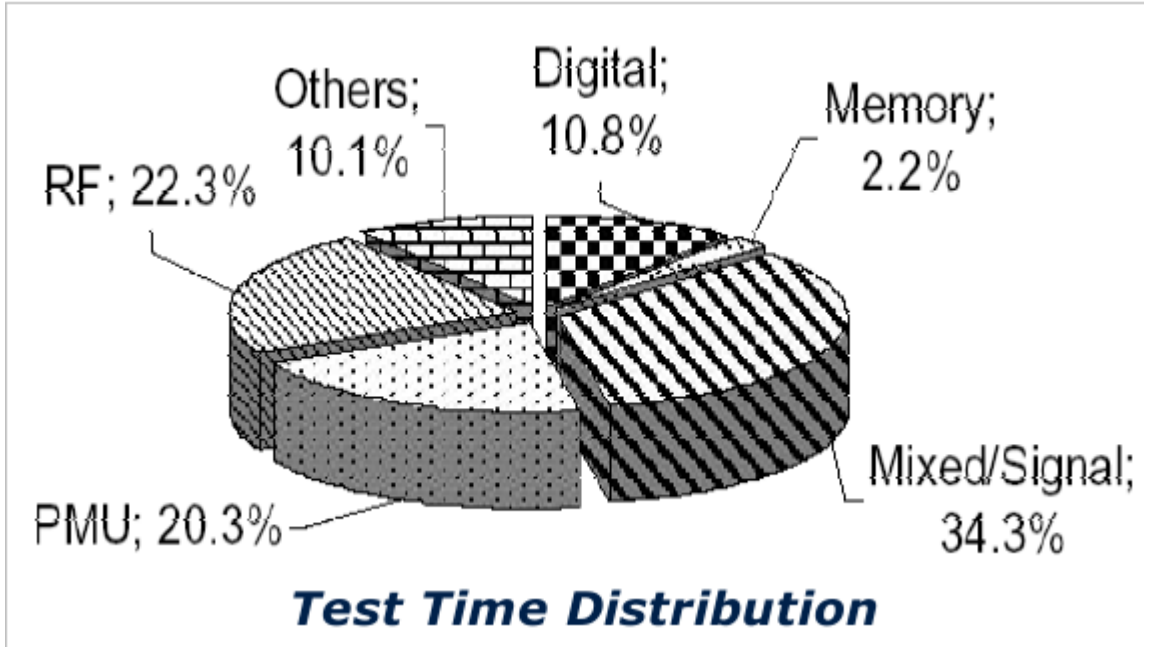
- Digital baseband, CPU, DSP
- RF transceiver, FM radio
- Audio processing
- Power management unit
- Interfaces for camera, USB, keypad



Analog:
30% area

To compare: Test time distribution for a mobile SoC device RF, AMS and PMU dominating

- Less than 15% contribution by digital tests
  - Scan tests for std. logic
  - BIST based memory tests
  - Functional performance tests
- Mixed-signal and RF tests drive
  - Production test time
  - ATE requirements
  - Test development cost
- Two test insertions
  - Wafer test (digital ATE)
  - Package test (SoC ATE)
- Wafer test insertion
  - Limited to basic digital tests
  - Room Temp only



Analog:
30% area
70% test time

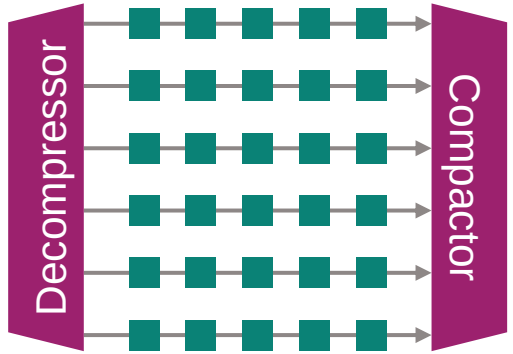
Classification of tests and typical measures applied

Class	Characteristic	Typical structure or module	Test or DfT measure
A	Long test time w/o significant ATE resource usage ('Wait')	NVM, DRAM	High test parallelism
B	Minor ATE resource requirements	Memory BIST	Candidates for on-chip concurrency
C	Data intensive	Scan test	On-chip compression, Logic BIST
D	High measurement accuracy needed at ATE	Analog-mixed signal parameter tests and trimming	On-chip measurements and BIST concepts

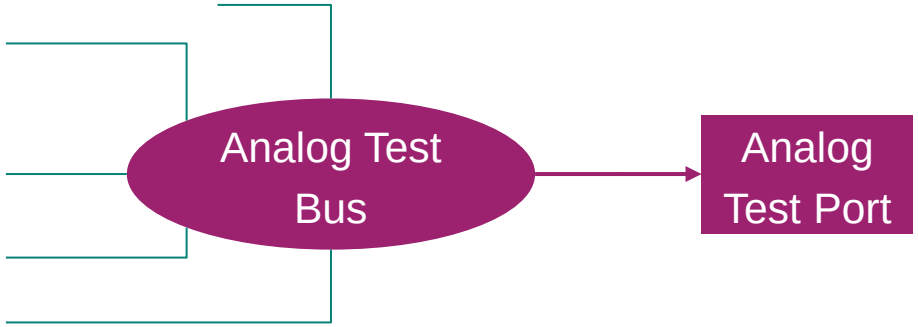
Let’s discuss the teamwork between test and DfT

Memory BIST

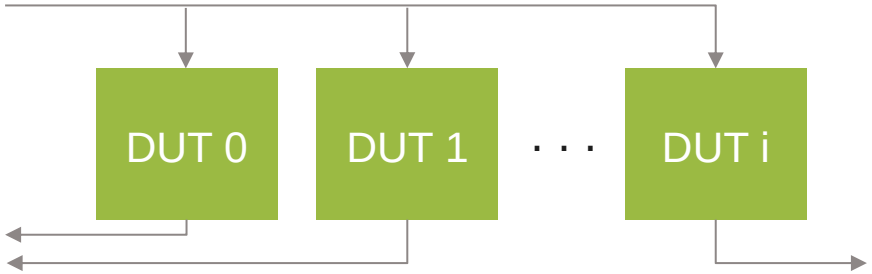
Scan test



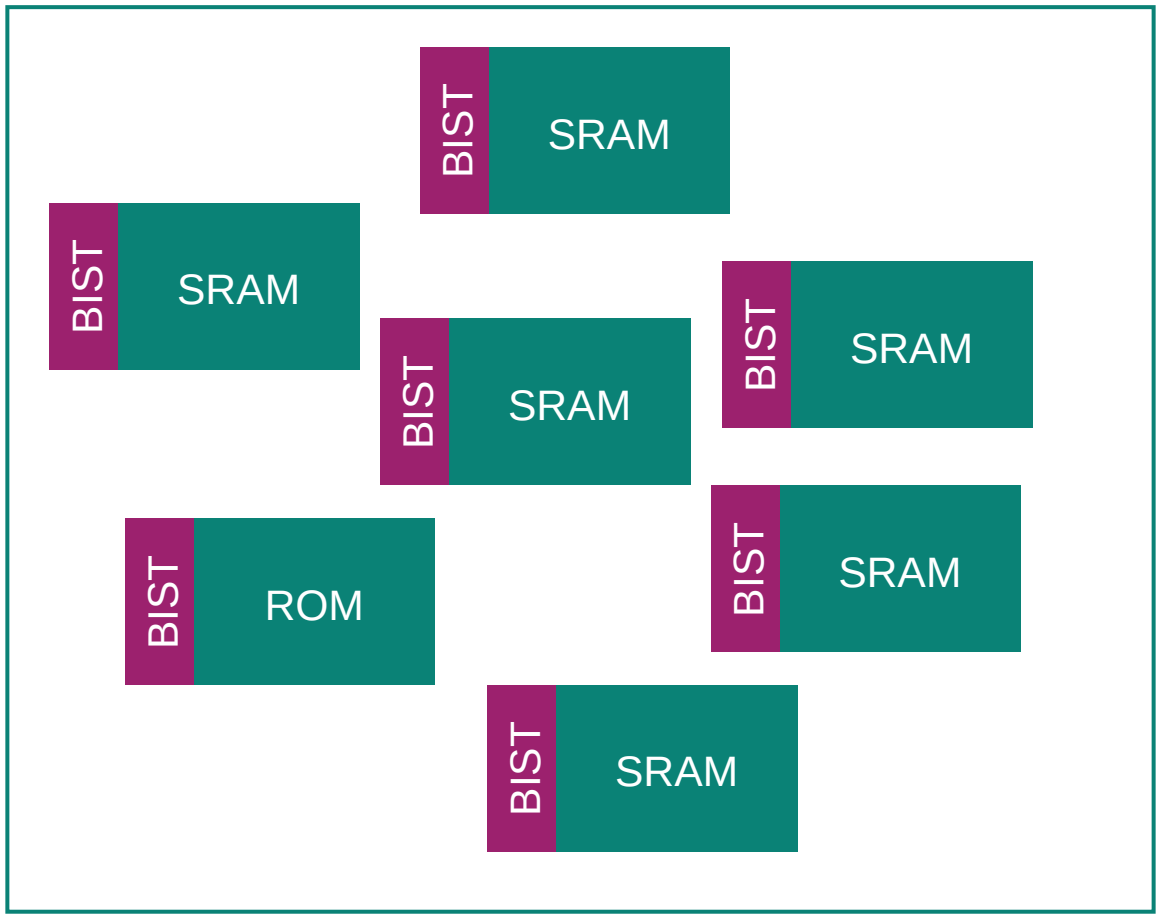
Analog mixed-signal tests



Multi-site test



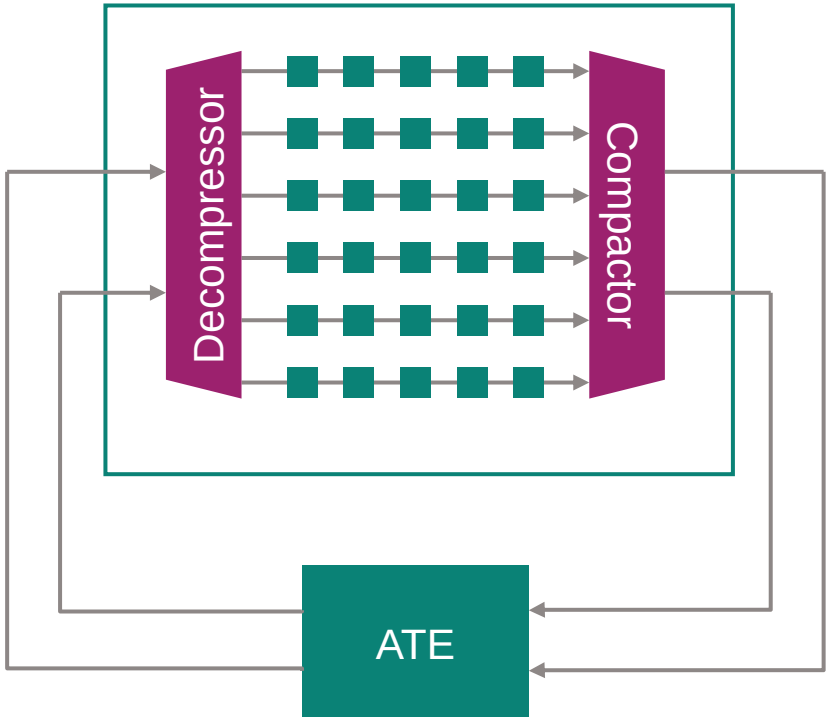
Test of embedded SRAM and ROM instances by Built-In Self-Test



- BIST enables concurrent test
  - Test algorithms implemented into BIST circuitry
  - Direct access to address and data of SRAM
  - Concurrency limited by power
- ATE-driven test (would have) access issues and no concurrent test option
- Highly automated implementation enabled by EDA tools
  - Including verification and pattern generation
  - BIST controller sharing to save area

On-chip scan compression reduces scan test time by 100x

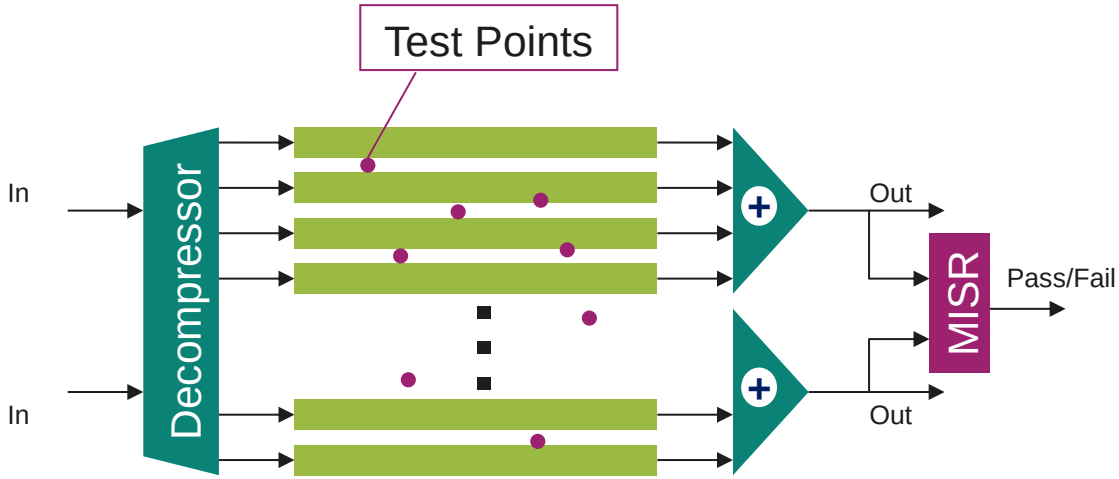
- On-chip compression logic reduces
  - Test time for scan by 100x
  - ATE vector memory requirement by 100x
- ATE investment saved
- Reflecting Moore‘s law
  - Doubling complexity every ~2 years
  - Complexity increase after 7 generations >100x
  - Scan compression saved investments for 7 generations or 14 years

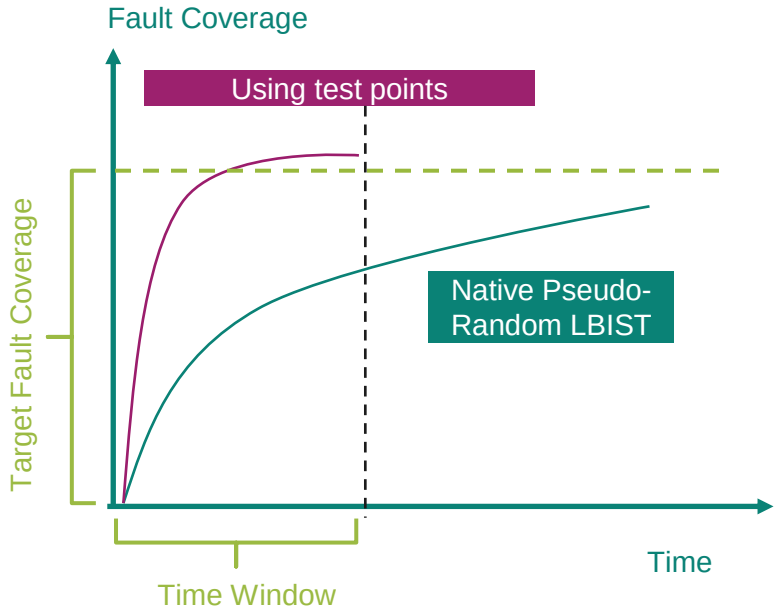


Logic Built-In-Self-Test (LBIST): Coverage limited by pseudo-random pattern

- Re-use of existing scan compression architecture
  - Hierarchical scan approach (‚Partitions‘)
  - Compression architecture enhanced by multiple-input signature register (MISR)
  - Isolation of partitions (no ‚X‘ capturing)

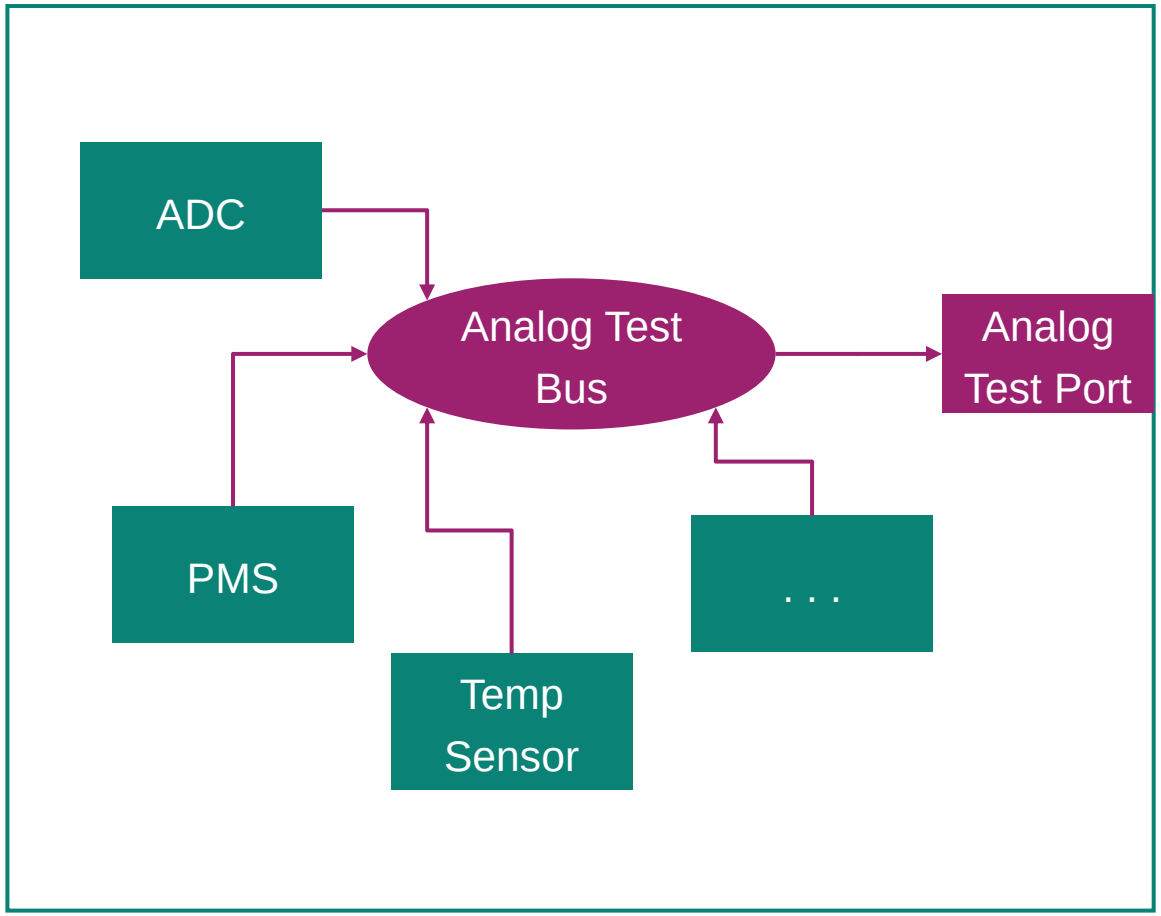
- Coverage limited by pseudo-random pattern
  - Hard to achieve coverages of 95%
  - Test points used to get target coverage within available time





Analog mixed-signal test is (almost) about measuring

- Every spec parameter needs confirmation with certain accuracy
  - ATE requires corresponding capabilities
  - Typically, subset of spec parameters measured during manufacturing test
- Trimming to compensate for die-to-die variations



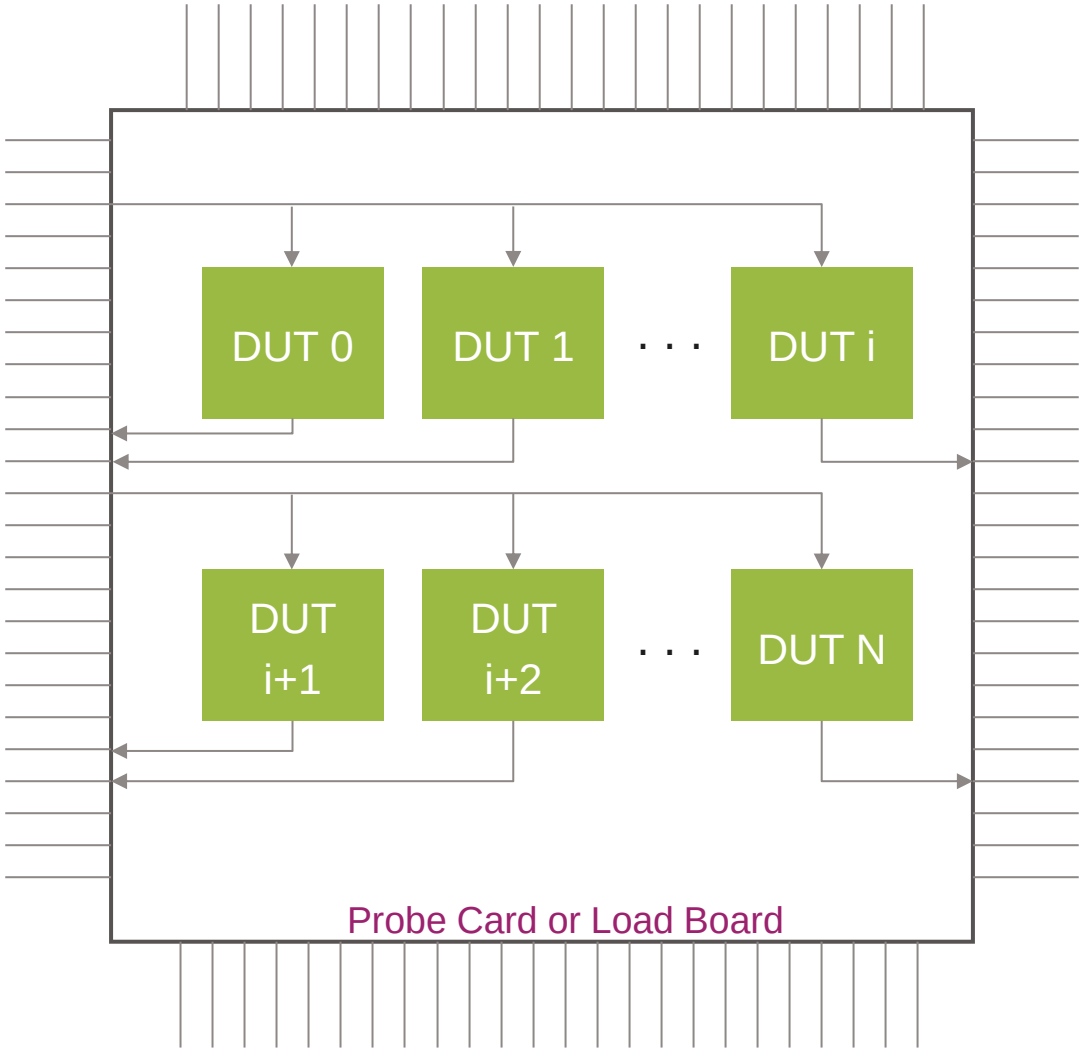
Multi-site test: Improve test time by factors

- ATE might have unused channels
- Input channels can be broadcasted

- Wafer test with reduced pin count and test set to achieve higher parallelism

- More expensive ATE HW than single site

- Limits
  - Power supply
  - Needle pressure



Summary on teamwork's output

Memory BIST

- Perfect example to overcome access problems
- Enables on-chip parallelism
- Limited by power supply only

Scan test

- Highest data volume for ATE
- Scan compression delivers a reduction by 100x
  - Available since 2000
  - Saved us ~7 technology generations
- Logic BIST on top of scan compression
  - Hard to achieve coverages > 95%

Analog mixed-signal tests

- Required measurements accuracy depends on
  - Product specification
  - Trimming needs
- Typically defines ATE price tag

Multi-site

- Standard today, more complex test hardware
- Wafer test
  - Higher parallelism
  - Reduced pin count
- Device test
  - All pins contacted

Who sets the direction?

Who sets the direction?
There is a common target and all contribute
We need innovative steps at both side of the bridge

#bestplacetobeindft