# 4th Workshop on Intelligent Methods for Test and Reliability

May 28-29, 2026, Chania, Crete, Greece

# Technical Program

## Thursday, May 28

**16:30 Introduction to the Workshop**
*Dirk Pflüger, Matthias Sauer, Matteo Sonza Reorda, Hussam Amrouch, Krishnendu Chakrabarty, Said Hamdioui, Ilia Polian (U Stuttgart, DE, Advantest Europe, DE, Politecnico di Torino, IT, TU Munich, DE, Arizona State U, US, TU Delft, NL)*

**16:35 Invited talk Steve Sunter, Siemens EDA**

**Title:** Testing A/MS Circuits More Intelligently

**17:20 Break**

**17:30 Session 1: Analog/Mixed-signal Circuits and RF**

Uncertainty-Guided Live Measurement Sequencing for Fast Real-Time ADC Linearity Testing
*Thorben Schey, Khaled Karoonlatifi, Michael Weyrich and Andrey Morozov, U Stuttgart, Advantest*

TBA
*Viet-Dung Nguyen, Jose Moreira, Jan Hesselbarth, U Stuttgart, Advantest*

**18:30 Invited talk Srinivas Vooka, Google**

**Title:** Beyond the ATE: Repurposing DFT as a High-Resolution Forensic Engine for the AI Era

**19:30 Reception**

## Friday, May 29

**8:45 Invited talk Martin Keim, Siemens EDA**

**Title: Design-for-Test considerations for AI designs**

**9:30 Session 2: System-Level Test and 3D ICs**

An Open-Source Power Measurement Platform for System-Level Semiconductor Testing
*Linus Bantel, Sarah Rottacker and Dirk Pflüger*, U Stuttgart, Advantest

Power-aware System-Level Test Program Generation for Chiplet-Based 3D ICs
*Denis Schwachhofer, Jennifer Dworak, Steffen Becker, Stefan Wagner, Matthias Sauer, Ilia Polian, U Stuttgart, SMU, TU Munich, Advantest*

**10:30 Coffee Break**

**11:00 Invited Talk Abhijit Chatterjee, School of ECE, Georgia Institute of Technology, Atlanta, GA**

**Title:** Using AI to Test AI Circuits and Digital Elements

**11:45 Session 3: Security and Reliability around the DUT**

Secure Multiparty Computation for Machine Learning-Based Semiconductor Testing
*Andreas Glinka, Ralf Küsters, Marc Rivinius, U Stuttgart, Advantest*

Analytics Driven Intelligent Device Tester Calibration
*Anand Venkatachalam, Ernst Aderholz, Matthias Sauer, Simon Schweizer, Matthias Werner and Ilia Polian, U Stuttgart, Advantest, Infineon*

**12:45 Lunch break**

**14:30 Session 4: AI-based Techniques for Testing and Modeling**

TBA
*Tarek Mohammed, Hussam Amrouch, U Stuttgart, TU Munich*

Physics-Guided Interpretable Modeling of Ring Oscillator Characteristics Under Bias Variations
*Yang Yang, Yiwen Liao and Bin Yang, U Stuttgart, Advantest*

On-Chip Sensing and On-Chip Learning for Performance Tuning of Mixed-Signal ASICs
*Tim Strobel, Sarah Rottacker, Roland Rösslhuber and Jens Anders, U Stuttgart, Advantest*

**16:00 Workshop Wrap Up**

# Abstracts of Invited Talks and Biographical Sketches of the Speakers

**Steve Sunter, Siemens EDA**

***Abstract*** – At this Workshop last year, it was observed that scan test has become the dominant test method for digital circuits, but system-level test (SLT) is still needed, and that A/MS tests can dominate total test time for ICs. Testing a large number of functional specifications for each analog circuit is becoming impractical, especially if their defect coverage is unknown and it is impractical to measure it via simulation. Analog scan test was recently proposed as an alternative to functional test. It offers a way to achieve the efficiency and simplicity of digital scan, but can it replace analog functional testing? If not, why not, and if it can, what are the consequences? In any case, what opportunities does analog scan testing provide for AI? Answers to these questions lead to a conclusion about a more intelligent way to test A/MS circuits.

***Bio***

*Steve has been working in mixed-signal IC design, test, and design-for-test (DfT) for almost 50 years. He is lead author of over 50 papers (5 of which won ITC Best Paper or Honorable Mention awards) and two dozen US patents on these topics, and co-author/inventor of many others. He has been an Editor of JETTA for over 10 years, an ITC Program Committee member for over 15 years, and a VTS Program Committee member for over 30 years. He is Chair of the IEEE P1687.2*

*Working Group and was a Chair of the P2427 Working Group, thrice a Program Chair of the Mixed-Signal Test Workshop (IMSTW), and a Vice-Chair of the P1149.4 WG. At Siemens EDA, formerly Mentor Graphics, he is the Engineering Director for Mixed-Signal DfT, a position he has held for 30 years.*

**Martin Keim, Siemens EDA**

**Abstract** – Three-dimensional multi-die AI devices cause numerous new Design-for-Test (DFT) requirements and opportunities, far beyond the classical Known-Good-Die needs. In this talk, we start at the end with the requirements for in-system online testing, monitoring, security & reliability, and others, for such a packaged device in its functional environment. We then follow these requirements all the way down to a core in a chiplet uncovering on the way how DFT ensures quality at each step and adds value throughout.

**Bio**

Dr. Martin Keim joined the Tessent product group of Mentor Graphics in 2001, now part of Siemens EDA, where he is Senior Engineering Director responsible for Memory Testing, Built-In Self-Test Diagnosis products, IJTAG, as well as Multi-die testing. Dr. Keim is a past member of the IEEE 1687-2014 working group, past secretary of IEEE P1687.1, member of the IEEE P3405, P1838a, and P1687.1 working groups, general chair of the current P1687 Refresh working group, and secretary of IEEE's Test Technology Standards Committee. He holds several national and international patents and is author of numerous technical publications. He received a doctorate in Informatics from the Albert-Ludwigs University in Freiburg im Breisgau, Germany.

**Abhijit Chatterjee, School of ECE, Georgia Institute of Technology, Atlanta, GA**

**Abstract -** Recent trends in AI for edge and IoT applications are increasingly dominated by power consumption constraints forcing designers to pick analog electronics for matrix-vector computations. Such analog elements, namely analog crossbars, are vulnerable to manufacturing process variations and defects, and are impacted by the resulting loss of manufacturing yield. To address this, we propose using AI algorithms and techniques to both detect and correct defective analog crossbar based AI systems ranging from deep neural networks and language models to generative adversarial networks. At the same time, AI systems also suffer from "mercurial digital cores" that produce irreproducible errors making testing of digital subsystems difficult. In this context, the cell-aware standard cell testing methodology that has evolved to detect subtle timing errors in digital circuits, is a great step forward but suffers from extensive fault simulation complexity. To address this, we present a novel AI -assisted fault simulation and grading framework that offers up to 10,000X reduction in fault simulation effort of large standard cell libraries with minimal impact on fault coverage. Test cases and simulation results will be presented.

**Bio**

Abhijit Chatterjee is a Professor in the School of Electrical and Computer Engineering at Georgia Tech and a Fellow of the IEEE. He received his Ph.D in electrical and computer engineering from the University of Illinois at Urbana-Champaign in 1990. Dr. Chatterjee received the NSF Research Initiation Award in 1993 and the NSF CAREER Award in 1995. He has received seven Best Paper Awards and three Best Paper Award nominations. His work on self-healing chips was featured as one of General Electric's key technical achievements in 1992 and was cited by the *Wall Street Journal*. In 1995, he was named a Collaborating Partner in NASA's New Millennium project. In 1996, he received the Outstanding Faculty for Research Award from the Georgia Tech Packaging Research Center, and in 2000, he received the Outstanding Faculty for Technology Transfer Award, also given by the Packaging Research Center. In 2007, his group received the Margarida Jacome Award for work on VIZOR: Virtually Zero Margin Adaptive RF from the Berkeley Gigascale Research Center (GSRC). Dr. Chatterjee has authored over 475 papers in refereed journals and meetings and has 22 patents. He is a co-founder of Ardext Technologies Inc., a mixed-signal test solutions company and served as chairman and chief scientist from 2000-2002. His research interests include error-resilient signal processing, control systems and AI architectures, mixed-signal/RF/multi-GHz design and test and adaptive real-time systems.

**Srinivas Vooka, Google**

**Abstract** – For fifty years, Design for Test (DFT) was defined by the 'Go/No-Go' result of the manufacturing line. As we enter the next decade, this definition is becoming incomplete. As chips transform into massive, heterogeneous AI ecosystems and software stacks grow, the primary bottleneck is no longer just confirming that we manufactured the silicon right, but also understanding '*why the SoC is behaving the way it is*.' This keynote presents a vision for 2026–2036, where DFT—in addition to its roles in defect detection and yield improvement—adds the critical application of serving as a System-Level Diagnostic Engine.

**Bio**

*Srinivas Vooka leads the global Silicon Design-for-Test (DFT) team at Google, bringing over two decades of deep experience in DFT and System-on-Chip (SoC) Design Management. A recognized expert in the field of DFT, Srinivas has authored or co-authored multiple IEEE papers & patents, delivered invited talks. Their career highlights include successfully leading cross-functional teams from architecture to product engineering, demonstrating a strong blend of technical acumen and project leadership.*