## 2nd Workshop on Intelligent Methods for Test and Reliability

May 25-26, Venice, Italy

# Technical Program

## Thursday, May 25

**16:00 Introduction to the Workshop**
*Dirk Pflueger, Matthias Sauer, Matteo Sonza Reorda, Hussam Amrouch, Krishnendu Chakrabarty, Said Hamdioui, Ilia Polian (U Stuttgart, DE, Advantest Europe, DE, Politecnico di Torino, IT, TU Munich, DE, Duke U, US, TU Delft, NL)*

**16:10 Invited talk Jennifer Dworak**

Why Should DFT Stop at Test? Reusing DFT in Functional Mode
*Alexander Coyle, Hui Jiang, Jennifer Dworak, Theodore Manikas, and Kundan Nepal*

**16:40 Panel**
Emerging Technologies: Seamless Integration or long Journey of Adaptation?
*Organizer: Hussam Amrouch (U Stuttgart, DE and TU Munich, DE)*
*Panelists: Said Hamdioui (TU Delft), Lilas Alrahis (New York U Abu Dhabi, UAE), Matthias Sauer (Advantest, DE), Abhijit Chatterjee (Georgia Tech, US)*

**17:40 Technical Papers**

QMESy: Towards Quality Measurement for Explanations in System Design
*Goerschwin Fey, Swantje Plambeck and Bernhard J. Berger, TU Hamburg-Harburg*

Multipars: Reduced-Communication MPC over $\mathbb Z_{2^k}$
*Sebastian Hasler, Pascal Reisert, Marc Rivinius and Ralf Küsters, U Stuttgart*

Maximizing Power Consumption by Exploiting Genetic Algorithms for Automatic System-Level Test Program Generation
*Denis Schwachhofer, Francesco Angione, Steffen Becker, Stefan Wagner, Matthias Sauer, Paolo Bernardi and Ilia Polian, U Stuttgart, Politecnico di Torino, Advantest*

**18:45 Reception**

## Friday, May 26

**8:30 Invited Talk Lilas Alrahis**

PoisonedGNN: Backdoor Attack on Graph Neural Networks-based Hardware Security Systems
*Lilas Alrahis and Ozgur Sinanoglu (New York U Abu Dhabi, UAE)*

**9:00 Poster Session: Projects of Graduate School Intelligent Methods for Test and Reliability**

(including 5-minute pitches)

Visual Analytics for Post-Silicon Validation
*Andrés Lalama, Thomas Ertl, Daniel Weiskopf, Steffen Koch (U Stuttgart, DE)*

Self-Learning Tuning for Post-Silicon Validation
*Peter Domanski, Dirk Pflüger (U Stuttgart, DE)*

Hyperdimensional Computing for Chip Testing -Towards Learning Fast from Little Data
*Paul Genßler, Hussam Amrouch (U Stuttgart, DE and TU Munich, DE)*

Online Evaluation of System Health State
*Hanieh Jafarzadeh, Hans-Joachim Wunderlich (U Stuttgart)*

Design for Testing and Reliability in the Presence of Transistor Self-Heating for Advanced Technologies
*Florian Klemme, Hussam Amrouch (U Stuttgart, DE and TU Munich, DE)*

Secure and Privacy-Preserving Semiconductor Testing
*Sebastian Hasler, Ralf Küsters (U Stuttgart, DE)*

Systematic Analysis of System-Level Test Fails
Nourhan Elhamawy, Jens Anders, Ilia Polian *(U Stuttgart, DE)*

Automated Generation of System-Level Test Programs for Characterization of Parametric Device Properties
*Denis Schwachhofer, Ilia Polian, Stefan Wagner, Steffen Becker (U Stuttgart, DE)*

**10:00 Coffee Break**

**10:30 Session 2: Joint session with AI-Treats**

**12:30 Lunch**

**13:30 Keynote Yervant Zorian**

Title TBD
*Yervant Zorian (Synopsys, US)*

**14:15 Keynote Georges Gielen**

Improving defect coverage for analog/mixed-signal ICs: machine learning to the rescue
*Georges Gielen (KU Leuven, BE)*

**15:00 Invited Talk Stefan Holst**

Tackling Test and Diagnosis Challenges Using GPU-Based High-Throughput Timing Simulation
*Stefan Holst (Kyushu Insititute of Technology, JP)*

**15:30 Workshop Wrap Up**