1st Workshop on Intelligent Methods for Test and Reliability

May 26-27, Barcelona, Spain

Technical Program

Thursday, May 26

16:00 Introduction to the Workshop
Dirk Pflueger, Matthias Sauer, Matteo Sonza Reorda, Hussam Amrouch, Krishnendu Chakrabarty, Ilia Polian (U Stuttgart, DE, Advantest Europe, DE, Politecnico di Torino, IT, Duke U, US)

16:15 Keynote 1
Enabling On-Chip Big Data Collection for Test and Reliability
Artur Jutman (Testonica, Tallinn, EE)

17:05 Session 1: Secure and Reliable Computations

Tiled ABFT for GEMM in SIMD Processors
Sandeep Bal, Chandra Sekhar Mummidi, Brunno F. Goldstein, Sudarshan Srinivasan, Sandip Kundu (UMass Amherst, US, U Federal de Rio de Janeiro, BR, Intel Bengaluru, IN)

Privacy-Preserving Computation in the Semiconductor Production Chain
Sebastian Hasler, Georg Karich, Ralf Küsters, Pascal Reisert and Matthias Sauer (U Stuttgart, DE, Advantest Europe, DE)

Brain-Inspired Hyperdimensional Computing for Semiconductor Test and Reliability
Paul R. Genssler and Hussam Amrouch (U Stuttgart, DE)

18:45 Reception

Friday, May 27

8:30 Keynote 2
Reliability and Robustness of Neuromorphic Computing: Approaches for RRAM Crossbars and Optical Neural Networks
Ulf Schlichtmann (TU Munich, DE)

9:20 Panel
ML for Test from Theory to Practice: Are We Ready?
Moderator: *Hussam Amrouch*
Panelists: *Matthias Sauer (Advantest), Ulf Schlichtmann (TUM), Mehdi Tahoori (KIT), Dirk Pflüger (Uni Stuttgart)*.

10:30 Coffee Break

11:15 Session 2: Test of Microprocessors and Deep-Learning Hardware

Efficient Low Cost Alternative Testing of Analog Crossbar Arrays for Deep Neural Networks
Kwondo Ma, Anurup Saha, Chandramouli Amarnath, Abhijit Chatterjee (Georgia Tech, US)

Covering the Long Tail Test Patterns by System-Level Test
Nourhan Elhamawy, Jens Anders, Ilia Polian, Matthias Sauer (U Stuttgart, DE, Advantest Europe, DE)

Automating Greybox System-Level Test Generation using Fuzzing
Denis Schwachhofer, Maik Betka, Steffen Becker, Matthias Sauer, Stefan Wagner, Ilia Polian
(U Stuttgart, DE, Advantest Europe, DE

12:45 Lunch

14:00 Keynote 3

Security of Test and ML for Test
Ramesh Karri (New York U, US)

14:50 Session 3: Intelligent Techniques for Post-Silicon Validation

An interactive visualization workflow for debugging in post-silicon validation
Andres Lalama, Johannes Knittel, Steffen Koch, Sarah Rottacker, Raphaël Latty, Jochen Rivoir, Thomas Ertl (U Stuttgart, DE, Advantest Europe, DE)

Mitigating the Complexity of Chip Designs with ML-based Cell Library Characterization
Florian Klemme and Hussam Amrouch (U Stuttgart, DE)

Conditional Variable Selection for Intelligent Test
Yiwen Liao, Tianjie Ge, Raphaël Latty and Bin Yang (U Stuttgart, DE, Advantest Europe, DE)

16:20 Workshop Wrap Up