Developing of Ultra-Wideband and High Linear Power Amplifiers in a 22nm FD-SOI CMOS Technology

Milestone Report of P7 INWAVE – GS-IMTR

Athanasios Gatzastras

October 4, 2022

Advisor / main examiner: Prof. Dr.-Ing. Ingmar Kallfass

Co-examiner: Jun.Prof. Dr.-Ing. Hussam Amrouch

Mentor: Dr.-Ing. Christian Volmer

Contents

1 Introduction

This milestone report presents the current status of project P7: Miniaturized Millimeter-Wave RF Interface Module (INWAVE), which is part of the Graduate School Intelligent Methods for Test and Reliability (GS-IMTR) of the University of Stuttgart. The project start was dated for January 2020 and is expected to finish in December 2022. Currently, a extension of this project until December 2023 is submitted to the Board of Directors.
The focus of INWAVE lies on the investigation and development of a millimeter-wave (mmw) interface module, which is able to provide ultra-wideband analog signals to a device under test (DUT) for testing purposes. One goal of this project is to cover the entire frequency range from 16 GHz to 90 GHz to enable testing for applications such as 24 GHz Industrial, Scientific and Medical Band (ISM), wireless point-to-point links, or automotive radar from 77 GHz to 79 GHz.

1.1 The Vision

The system overview of the vision of INWAVE is depicted in Fig.1. The interface module should be designed to be coupled to the RF base card from Advantest and is composed of a transmitter (Tx), a receiver (Rx), a local oszillator (LO) multiplication, as well as a switch matrix at the inputs and outputs. INWAVE is focusing on the comparatively more challenging Tx-chain of this system.

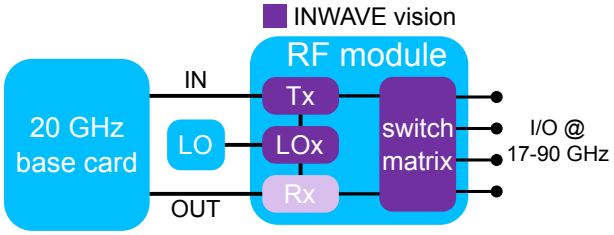


Figure 1: A system overview of a RF test interface

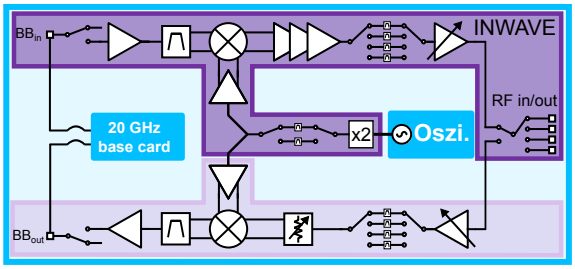


Figure 2: RF interface module detailed

A detailed schematic drawing of the interface module is depicted in Fig.2. It consits of many different building blocks like amplifiers, filters, switches, frequency multipliers and mixers. The vision of INWAVE and future projects is to design such a system with the requirements on the dynamic range and the frequency range as a single-chip solution.

1.2 First Steps

This chapter describes the first steps that were required to be taken at the beginning of this project. After a technology evaluation, the decision was made to use a state-of-the-art 22 nm fully depleted Silicon-On-Insulator (FD-SOI) complementary metal-oxide-semiconductor (CMOS) technologie provided by Globalfoundries in order to meet the demand of a compact system-on-chip (SoC). The plan was to implement first breakout components to verify the maturity of this process and the available simulation environment.

1.2.1 The 22nm FD-SOI CMOS Technology

The chosen 22 nm CMOS FD-SOI has the ability to combine both, complex digital, as well as analog circuits in the mmWave domain as one-chip solution [1]. With a transit frequency (f_t) of 353 GHz and a maximum frequency of oscillation (f_{max}) of 370 GHz this platform looks very promising for the requirements of this project. Furthermore the technology is characterized by an ultra-low leakage current and is thus a promising candidate for RF applications [2]. Additionally, the SOI approach opens up the ability to use an ultra-thin burried oxide (BOX) as a back-gate which allows several tuning options with respect to the transistors DC and high-frequency performance [3], [4]. A cross section of the transistor is shown in Fig.3. The used metal stack option contains 11 metal layer. The corresponding simplified metal stack of this platform is shown in 4. While the top-most metallization is built by aluminum, the lower

metal layers are formed by copper in order to reduce ohmic losses. While the top three layer LB, QB and QA are used for the RF routing, the lower metallization layers are used for the high density routing at transistor level.

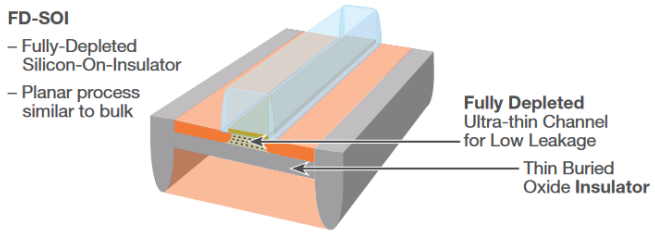


Figure 3: Cross section of a FD-SOI transistor. Source: https://www.globalfoundries.com /sites/default/files/product-briefs/pb-22fdx-soi-25-web.pdf

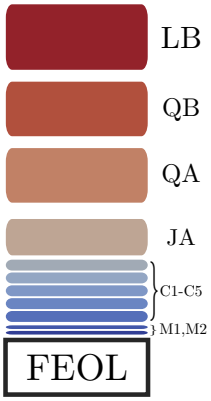


Figure 4: Simplified metal stack of the used option in this technology.

1.2.2 Simulation Environment

During the first year of this project, it was very important to establish the design and the entire tool-flow for this process. For this reason it was decided to focus at the beginnig on single breakout components of the system which are depicted in Fig.2. The goal was to verify on one hand the maturity of this process and on the other hand the available tools in the design environment.
Before starting the design phase, it is very important to ensure that the settings for all required analog RF simulations are under control and understood. The main performed simulations to meet the designgoals are:

- DC Bias sweeps
- Transient simulation
- Small-signal S-Parameter (SP)
- Large-signal S-Parameter (LSSP)
- Power sweeps
- Periodic Steady State (PSS)
- Envelope system simulation
- Noise simulation

Since the performance of the output amplifier is highly representative for the entire system performance, the focus of the first year was on designing an ultra-wideband power amplifier in this technology.

2 The First Iteration of the Amplifier Design

After a comprehensive analysis of different amplifier architectures by using the simulations mentioned above, the so-called travelling-wave amplifier (TWA) was selected for the first design. A TWA is characterized by an inherent ultra-wideband gain as well as input and output matching, simultaniously, which are very important parameters for this project.
An additional requirement from Advantest is that the amplifier should be true-differential in order to increase the dynamic range and to overcome common-mode issues. This hard requirement leads into a unique selling point for that kind of amplifier in the target frequency range up to 90 GHz.
A simplified schematic of the designed amplifier can be seen in Fig.5. The amplifier consists of seven uniform gain stages built by differential cascodes with a total power consumption of 230 mW. The concept of a TWA is to embed each gain stage into inductive transmission lines to form a so-called artifical transmission line with 50 Ω single-ended line impedance.

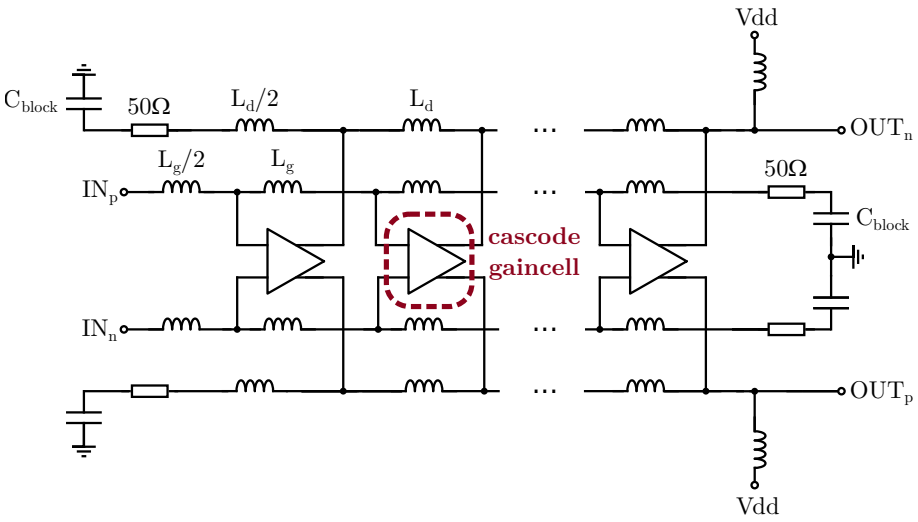


Figure 5: Simplified schematic view of the implemented fully differential travelling-wave amplifier.

The goal of those lines is to compensate the capacitive behaviour at the input and output of each gain cell to achieve a wideband impedance matching at the amplifier ports. Another important requirement for the transmission lines is the aimed constructive wave interference at each output of each gain element. The artificial transmission lines have to be designed in a way that the wave propagation at the gateline is equal to the one at the drainline. The requirements for the transmission lines regarding their length and impedance can be read in more deatil in[5].
Another requirement from Advantest is that the amplifier has to be DC-coupled to use this amplifier potentially as a buffer after a digital-to-analog converter (DAC) at system level. It should be noted, that the DC-feed network is realized on-chip by two RF-chokes at the drain lines of the amplifier, whereby no bulky external bias-tees are needed to use the amplifier. The detailed schematic and the corresponding layout in a 3D view are depicted in Fig.6 and Fig.7, respectively.
All selected transistors are *sltnfet* transistors, which are characterized by a super-low (sl) theshold voltage. Each transistor in the differential pair, formed by Q1-Q4 has a gate width of 12 µm, while the transistors in the current mirror Q5 and Q6 have a gate width of 75 µm. The comparatively large transistors in the current mirror are necessary to generate a DC current of 15 mA with a voltage drop of 200 mV over Q5. Fig.7 shows the zoomed layout of one gain cell in a 3D view. While the input lines are implemented on QB layer as microstrip lines with a ground pattern on M1 for area-optimized design, the output lines are implemented as coplanar lines on QA.

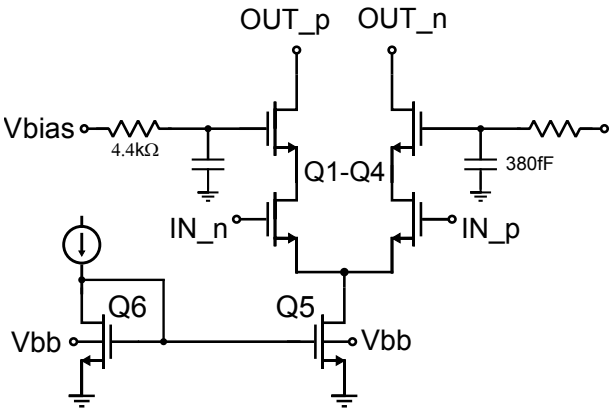


Figure 6: Schematic view of the designed differential gain cell.

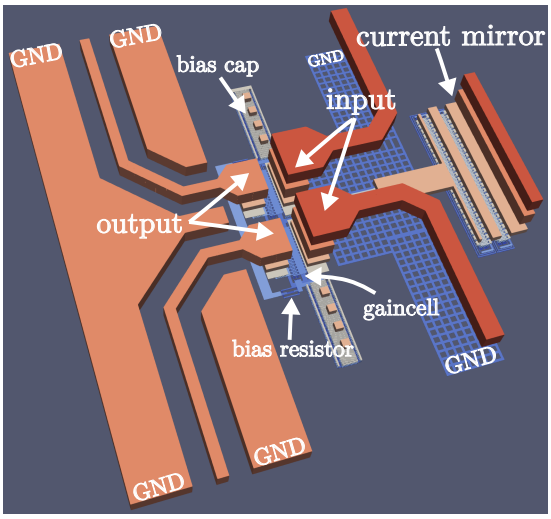


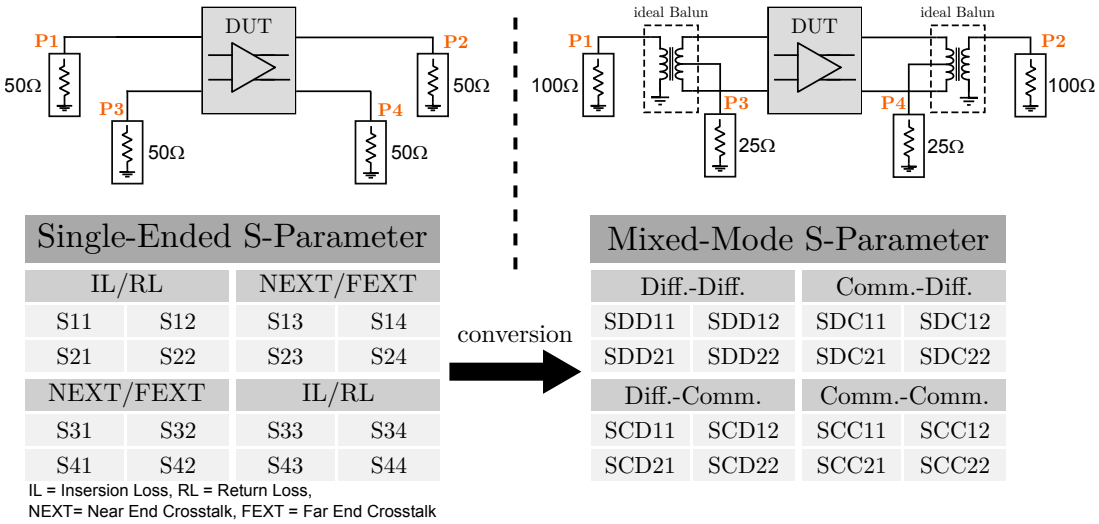
Figure 7: Simplified 3D layout view of the implemented gain cell.

Further details about the transmission line properties, the implementation, and the corresponding layout

can be seen in [5]. Important to notice at this point is that due to the limited tool capabilities for simulating the actual layout of such circuits properly from RF perspective the transmission lines and inductors are taken from the design library and simulated in the schematic view.

2.1 First Measurement Results

After one year design phase and after additional six months of fabrication and shipping, the first measurements could take place at the University of Stuttgart. The first measurement where performed with a four-port network analyzer up to 67 GHz provided by Advantest. For this measurement additional RF equipment had to be purchased. In order to be able to perform an on-wafer measurement inter alia two differential probes, cables with 1 mm coaxial connectors and the corresponding calibration substrate were ordered.
Fig.8 shows on the left-hand side how the measurement was performed and on the righ-hand side how the measured single-ended parameters can be transferred into the so-called mixed-mode S-parameter. The purpose of this parameter is to separate the measurement into a differential and into a common-mode behaviour of the circuit to get both independent of each other S-parameter matrices.



Single-Ended S-Parameter			
IL/RL		NEXT/FEXT	
S11	S12	S13	S14
S21	S22	S23	S24
NEXT/FEXT		IL/RL	
S31	S32	S33	S34
S41	S42	S43	S44

Mixed-Mode S-Parameter			
Diff.-Diff.		Comm.-Diff.	
SDD11	SDD12	SDC11	SDC12
SDD21	SDD22	SDC21	SDC22
Diff.-Comm.		Comm.-Comm.	
SCD11	SCD12	SCC11	SCC12
SCD21	SCD22	SCC21	SCC22

IL = Insersion Loss, RL = Return Loss,
NEXT= Near End Crosstalk, FEXT = Far End Crosstalk

Figure 8: Definition and interpretation of the measures S-parameter.

Fig.9 shows the even and odd-mode behaviour of the amplifier after the conversion of the single-ended to the mixed-mode matrix as shown in Fig.8. The results of the 4x4 mixed-mode S-parameter is reported in [5]. In comparison to the simulation an unusual mismatch for such a mature process between each parameter can be observed. Especially at lower frequencies up to 20 GHz the mismatch in the common and differental mode should not be as shown in the graph below.
Another odd thing was the DC characteristic of the amplifier that appears also in a breakout component on the chip. The investigation of the DC behaviour can be seen in *2021 Q3 P7 report* of INWAVE. There,

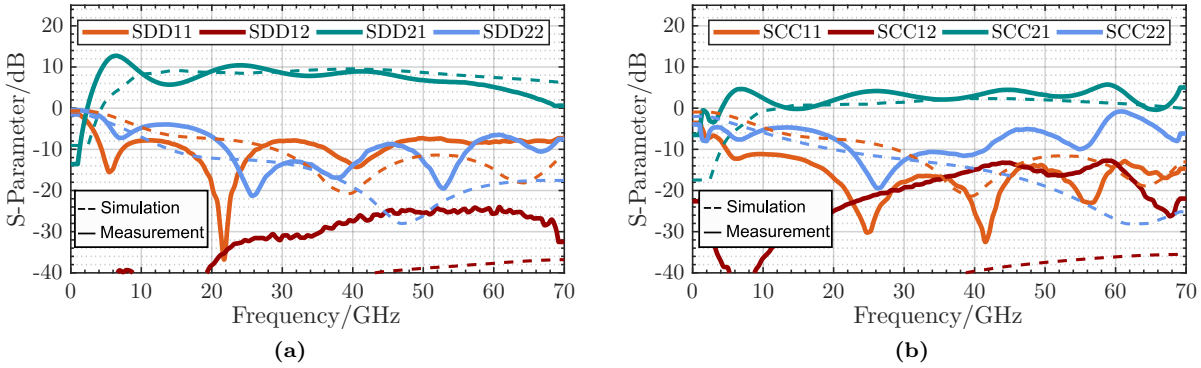


Figure 9: Measured differential mode S-parameter in (a) and common mode S-parameter in (b).

a mismatch of larger than 50% in the DC current of the gain cell was reported. This mismatch between the measurement and simulation could be eliminated by adding a resistor at the sources this differential pair on schematic level. Both, the mismatch in the high-frequency, as well as in the DC behavior are strong indicators for an incorrect simulation toolchain.

2.2 Conclusion of the First Iteration

In total it can be said that the first iteration of a power amplifier was successfull in terms of learned lessons. It was shown that the amplifier was working up to a frequency range from about 50 GHz with a gain of 6 dB and a peak gain of 12 dB. Simultaneously, a common-mode rejection up to 65 GHz was reached.
On the other hand, the findings can be summarized that the prediction in the simulation has urgently to be improved for the next iteration. The used simulation environment was not only inefficient in the design phase, but also inaccurate for this design. The plan before the re-design of the amplifier is first to enhance the prediction of the simulation with a more time-efficient simulation tool.

3 The Second Iteration of the Amplifier Design

This section describes the way to the second iteration of the proposed amplifier. The main goal of this phase was to find a way for a better prediction of the actual performance of the amplifier with a suitable simulation environment. The first measurements could be taken as a basis for a potential new simulation tool. After a more suitable simulation tool was found, the re-design of an amplifier could start.

3.1 Verification of EMX as New Simulation Engine

With the knowledge of the first iteration, the requirements for the new simulation are:

- full support by the foundry
- embeddable in the toolchain of Cadence
- suitable for mmW frequencies, as well for DC
- faster than the previous approaches
- possibility of simulating entire circuits
- compatible with DRC/LVS check
- high automation rate for max. efficiency

Following after an evaluation of different simulation tools, the decision for EMX as new simulation engine was made. EMX itself is a tool provided just recently at this time from Cadence and combines all mentioned requirements in one tool. The main reasons for selecting EMX are that it is completely supported by Globalfoundries, as well as from Cadence. Since additionally the simulation is much more efficient than other approached, EMX presents a promissing candidate for future designs.
After the initialization and first simulations with EMX, the plan was to re-simulate the entire implemented TWA and compare it with the measurements. Fig.10 shows how the amplifier can be re-simulated with EMX. On the left side the layout of the amplifier is shown. It can be seen, that the mesh covers the entire amplifier including the RF probe pads.
On the right side, the zoomed gain cell area and simultaneously one of the biggest advantages of EMX is shown. EMX has the ability to blackbox all transistors and lumped elements of the design automated and puts also automated simulation port at the device ports in the layout. This makes the simulation very time efficient, since the designer has only to set simulation ports at the top of the design hierarchy manually. This ability and the fact, that EMX is a 2.5D-simulator and thus optimized for planar processes, decrease the design and simulation time significantly and allow a very efficient design circle.
With this approach it was now possible to comprehend the measurement results of the first iteration.
Fig. 11 shows the DC measurement, the inital layout simulated with EMX, the prediction of the schematic view and simulation of the improved layout of this cell compared to each other. First, it can be seen that the re-simulation of the drain current matches now very good with the measurements. Furthermore, it can be observed in this graph, that the layout of this gain cell could be in that way enhanced that the drain current in the layout follows the prediction in the schematic view. The reason for this difference was the connection of the current source to the upper transistors, which was realized with a lower metal

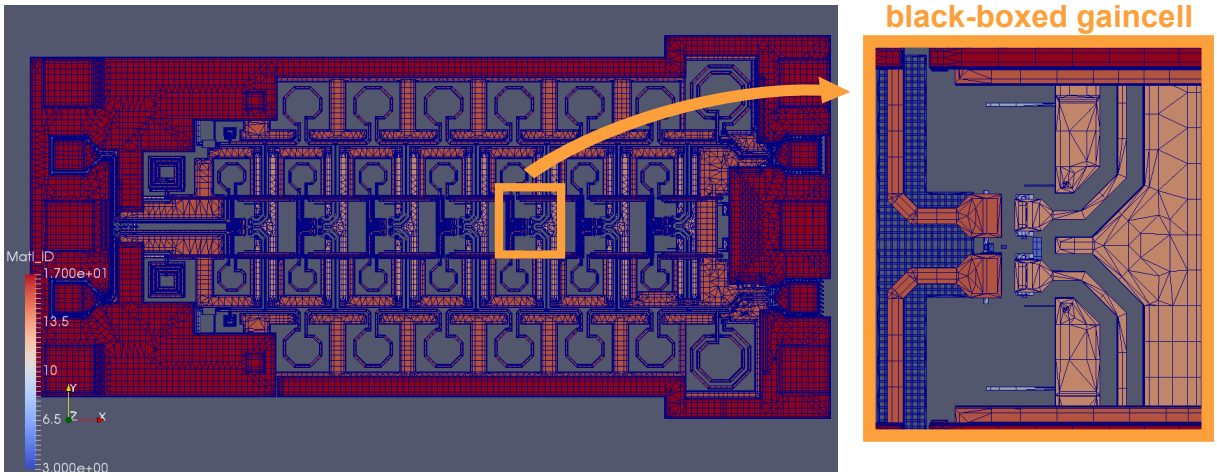


Figure 10: Entire TWA re-simulation with EMX

layer. This routing led to a high-ohmic connection in the DC-path and finally to the measured behavior. Conversely, this means that the sheet resistance was under-estimated by the tools used before.

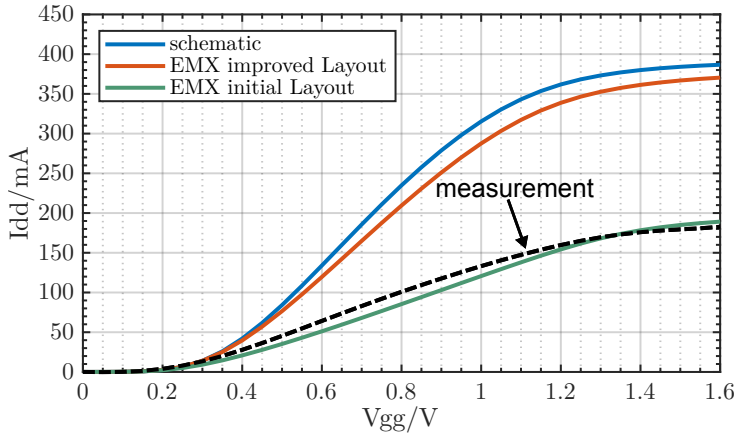


Figure 11: DC re-simulation of the stand-alone gain cell with EMX.

Fig.12 shows finally the results of the re-simulation of the entire TWA, as depicted in Fig.10. Although there is still a difference of partially a few dB at some frequencies in the amplitude of the S21, it can be said that the prediction of EMX is very good by considering also S11 and S22. An indicator is also the position of the zeros over the frequency. It can be observerd that for S11 and S22 the zeros lie with marginal difference at the same frequencies.

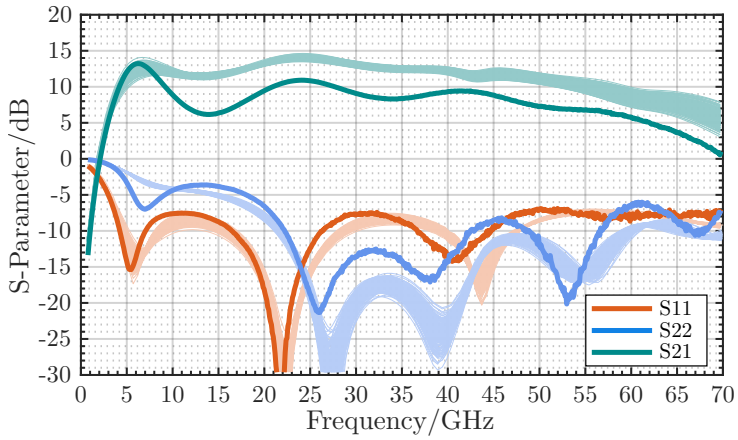


Figure 12: S-parameter Monte-Carlo re-simulation of the entire TWA with EMX.

3.2 Re-Design for the Second Iteration of the TWA

Based on the gained knowledge, the design for the second iteration of the amplifier can be proceeded with EMX as new simulation tool. The goals for the next implementation are an improved impedance matching at the in and output, an improved flat gain shape versus frequency and the replacement of the bulky inductors by transmission lines in the input and output path.
Fig.13 shows the layout of the entire layout of the second iteration. It consists of ten gain stages with a total length of roughly 1 mm. The bulky inductances could be now replaces as planned by transmission lines. Both DC feeds could now be shifted to the input of the amplifier in order to have only minor impact on the output. While the input gateline is designed on the top-most metal layer LB, the output drainline and the DC-feed inductors are formed by the metal layer QB. The reason for this configuration is simple the fact that LB has a ten-times higher resistivity that QB. The implementation of LB at the

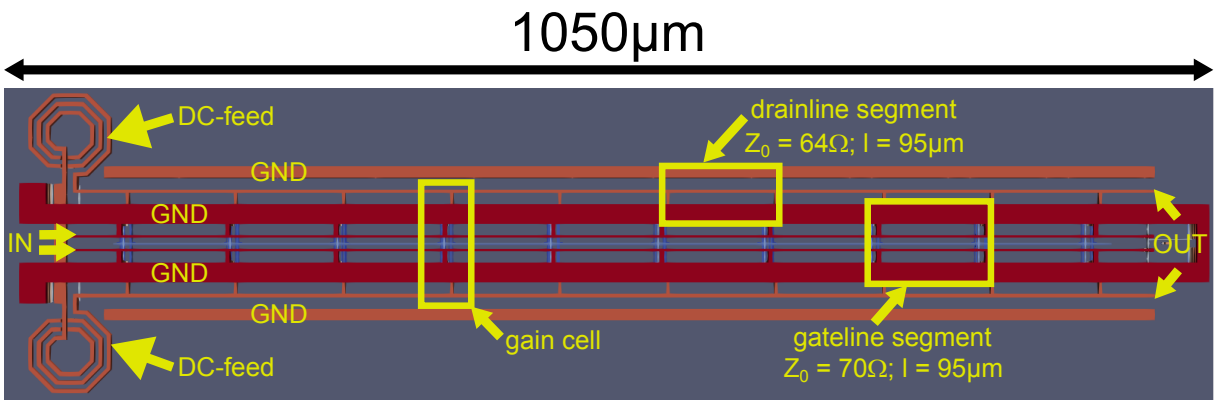


Figure 13: 3D Layout view of the second iteration of the proposed TWA.

drain line would lead to a high IR-drop and thus high DC-losses along the line. Since, the gate current is negligible small in this technology, the input lines can be realized on LB. Important to note is also, that the input lines, in contrast to the output lines, are implemented as differential coupled lines. The segments between each gain cell have a length of 95 µm. While the differential impedance of the gate line is 70 Ω, that of the drain line is 64 Ω.
Fig.14 shows the schematic and the corresponding layout of the redesigned gain cell. The biggest difference in the schematic to the gain cell in the first iteration is, that the current mirror is now replaced by Q5, which is beneficial for the routing in the toplevel of the chip. The DC bias current in the cell can be controlled by adjusting the voltage *V_current*, which is set to 530 mV and leads to a total current of 10.7 mA per cell. While Q1-Q4 have a gate width of 7 µm, Q5 is splitted into two transistors, as depicted in Fig.14b), with a gatewidth of 14 µm, each. In order to built a fully-differential amplifier, both parts of Q5 are connected via metal, which presents a virtual ground for the differential mode. This configuration allows a low-ohmic connection for each branch, since both parts of Q5 can directly be connected to higher

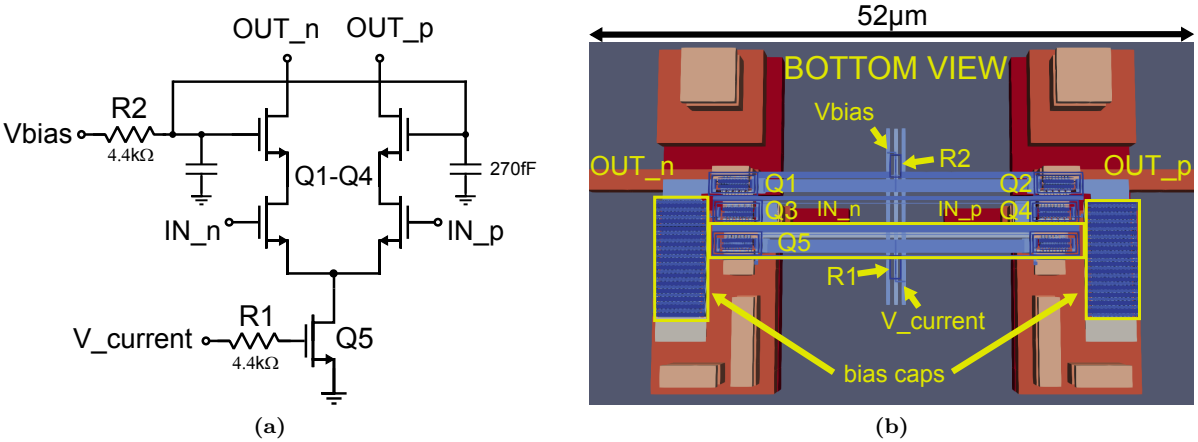


Figure 14: Schematic of the re-designed gain cell (a) and the corresponding layout in (b).

metallizations, which are simultaniously the ground lines for the RF signal shown in Fig.13. The lines for the bias voltages *V_current* and *Vbias* are arranged in that way that the connection to the following gainstage can be realized with a straight line, which simplifies the routing at the top-level.

3.3 Measurement Results

The second measurement campaign took place at Advantest and was splitted into two parts. The first part includes the 4-port fully differential measurements up to 67 GHz and for the the second part were single-ended measurements up to 110 GHz planned. The reported S-parameter are, as in Fig.8 shown, extracted.
The results of the first measurements are depicted in Fig.15. It can be seen, that the measurements match now very good with the simulation. The matching can not only be observed in the magnitude of each signal, but also in the phase of the signal in form of the plotted group delay of this amplifier in Fig15(d). Additionally, the position of the zeros in the common and in the differential mode match very good between the prediction of the simulation and the actual measurement. The amplifier reaches 12 dB peak gain and still 8 dB differential gain at 67 GHz. Not only the gain, but also the matching at the port of the amplifier could be much improved in comparison to the first version.

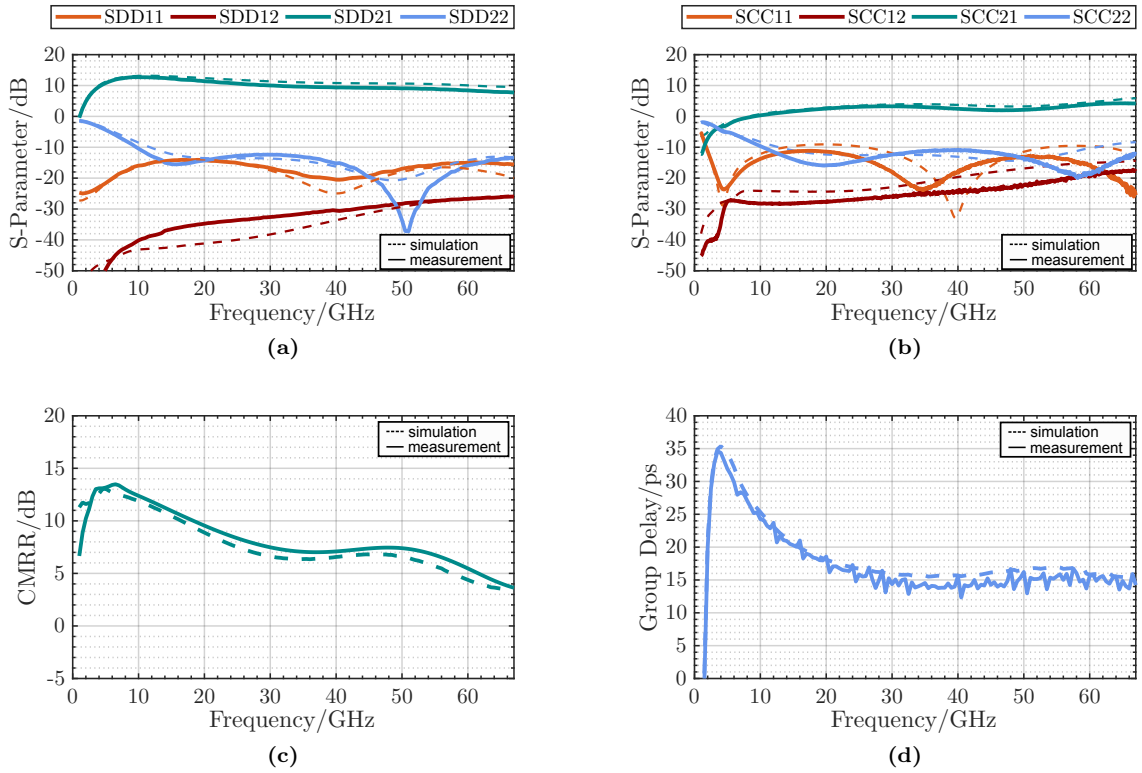


Figure 15: Measured differential mode S-parameter in (a), common mode S-parameter in (b), the CMRR in (c) and the group delay in (d) up to 67GHz.

The amplifier reaches a return loss of less than −10 dB from 10 GHz to 67 GHz at the input, as well as at the output. To be mentioned at this point is also the measured Common Mode Rejection Ratio (CMRR) which is the main purpose of using a fully differential amplifier. The CMRR reaches a peak of 13 dB at 6 GHz and is 5 dB up to 60 GHz.
Since these measurements were very promising, following measurements up to 110 GHz were focused. Since there is only one 2-Port Network Analyser (NWA) from Anritsu available for this measurements, an overview about the setup and the execution of the measurements and the calibration has to be reported. A simplified schematic of the measurement setup is shown in Fig.16. To be able to measure and get the most possible repeatability at both ports of each probe, a fixed setup of probe, cable and DC-Block was chosen. In this configuration, only the terminations and the the NWA modules have to be exchanged for the respective measurement. The calibration of this setup was in comparison the to one up to 67 GHz more challenging, since there is no differential calibration substrate available up to 110 GHz. This means

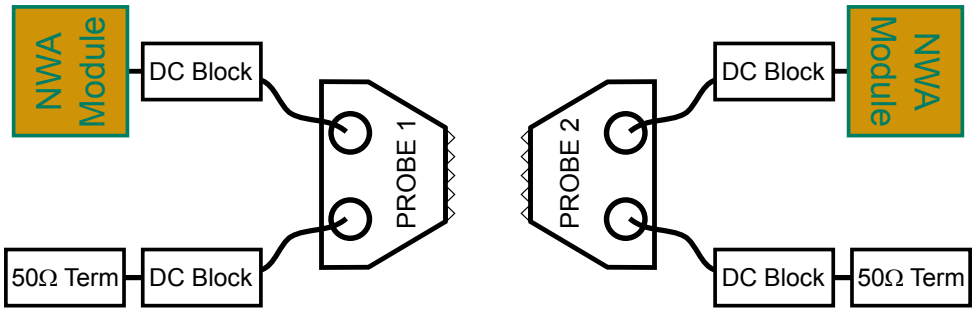


Figure 16: Measurement setup of the 110GHz measurement.

that for a full characterization of the amplifier a 2-port Short Open Load Through (SOLT) calibration has to be performed in four configurations as shown in Fig.17. For this purpose the valid assumption that the amplifier is perfectly symmetrical is made. The means that the measurements between P3 and P4 and P1 and P2 and the measurements between P1 and P4 and P3 and P4 are considered as identical, respectively.

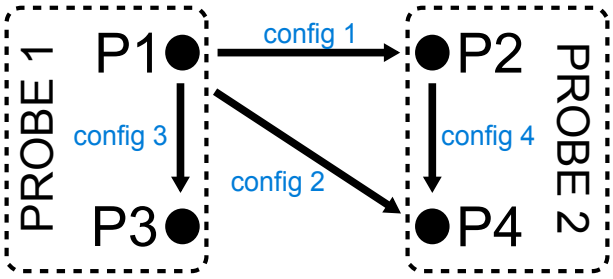


Figure 17: Calibration setup of the 110GHz measurement.

Fig.18 shows the performance of the TWA up to 110 GHz. In general it can be stated that the measurement results can be matched with the ones up to 67 GHz, which means, conversely, that the chosen 2-port calibration method used in this approach is valid. Furthermore, a good matching between simulation and measurement can be observed up to 110 GHz, which validates also the models provided by the foundry. The amplifier reaches 4 dB gain at 110 GHz and a return loss almost less than −10 dB from 10 GHz to 100 GHz at the output and over the entire frequency range of the measurement at the input. The CMRR follows also the prediction of the simulation and reaches 0 dB at 96 GHz. The group delay reaches a maximum ripple of 12 ps from 20 GHz to 110 GHz.

4 Conclusion and Outlook

Generally speaking the project until now can be considered as successful. Very important for the outcome of this project are the results from the latest measurements, which presented the world's first full-differential amplifier up to 110 GHz. It was also shown that the process is very suitable to realize the vision of the implementation of a Tx and Rx as single chip solution at the desired frequencies. The most important finding is the fact that a completely new platform and workflow is established, where it is now possible not only to design, but also to measure integrated circuit up to 110 GHz.
An key point for this possibilty was the implementation of EMX as simulation engine in the mmw domain after the gained knowledge of the first iteration. Also very important for the outcome of this project is, that at least for the small-signal analysis the models provided by Globalfoundries are very mature for those high frequencies which is absolutely not common in comparison to other Process Design Kits (PDKs) provided by other manufacturers.
The next step is now to perform many non-linear measurements and to continue the characterization of the implemented amplifier. Further measurements such as input power vs. output power vs. frequency differential up to 67 GHz, Adjacent Channel Power Ratio (ACPR) measurements for different modulation formats and communication standards vs. input power, Error Vector Magnitude (EVM) investigation for different modulation formats, eye-diagramm measurements for a 4 Pulse Amplitude Modulation (PAM4)

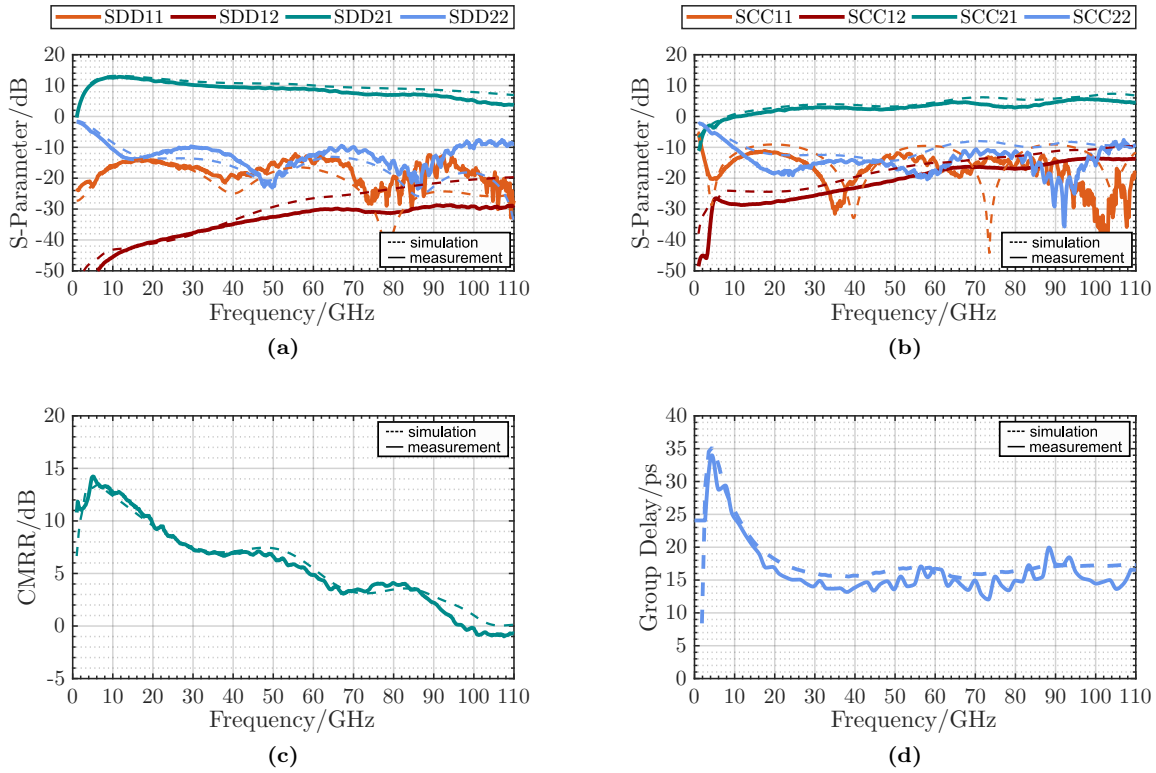


Figure 18: Measured differential mode S-parameter in (a), common mode S-parameter in (b), the CMRR in (c) and the group delay in (d) up to 110GHz.

and noise measurement are also planed. The first non-linear measurements will start at 18th of October 2022 at the facilities of Advantest. The first non-linear measurement will be power measurements at different frequencies to verify also the models in their non-linear behaviour.
Furthermore are at least one or maybe two iteration planed until the end of this project in 2023. Since, the models and the whole toolchain is verified, the next design phase can be tackled more confident. Planed is for example the implementation of a stacked amplifier cell in order to increase the dynamic range. Beyond that it is planed to improve the roll-off of the gain over frequency. An ideal TWA would have a very flat gain response over frequency and will drop abrupt at the wanted frequencies. To overcome also problems at system level the best solution for an amplifier would be one with a positive gain slope over frequency to overcome for example the rising insertion losses from passive components like cables in such a huge system as a test machine. First simulations to achieve a positive gain slope of the amplifier up to 90 GHz are already performed on schematic level and look very promising for the next design iteration.
Furthermore, it is planed to publish the latest measurement results in form of one or two journal papers and some breakout aspects in conference papers. The next conference submission is planed for the International Microwave Symposium (IMS), which is the biggest conference in the RF and mmw domain. The deadline for submitting a paper is the 6th of December 2022.

List of Abbreviations

INWAVE Miniaturized Millimeter-Wave RF Interface Module

GS-IMTR Graduate School Intelligent Methods for Test and Reliability

mmw millimeter-wave

DUT device under test

ISM Industrial, Scientific and Medical Band

SoC system-on-chip

Tx transmitter

Rx receiver

LO local oszillator

FD-SOI fully depleted Silicon-On-Insulator

CMOS complementary metal-oxide-semiconductor

TWA travelling-wave amplifier

BOX burried oxide

DAC digital-to-analog converter

CMRR Common Mode Rejection Ratio

NWA Network Analyser

SOLT Short Open Load Through

PDKs Process Design Kits

OP1dB output related 1-dB compression point

ACPR Adjacent Channel Power Ratio

EVM Error Vector Magnitude

PAM4 4 Pulse Amplitude Modulation

IMS International Microwave Symposium

References

[1] S.N. Ong, S. Lehmann, W.H. Chow, C. Zhang, C. Schippel, L.H.K. Chan, Y. Andee, M. Hauschildt, K.K.S. Tan, J. Watts, C.K. Lim, A. Divay, J.S. Wong, Z. Zhao, M. Govindarajan, C. Schwan, A. Huschka, A. Bcllaouar, W. LOo, J. Mazurier, C. Grass, R. Taylor, K.W.J. Chew, S. Embabi, G. Workman, A. Pakfar, S. Morvan, K. Sundaram, M. T. Lau, B. Rice, and D. Harame. A 22nm fdsoi technology optimized for rf/mmwave applications. In *2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 72–75, 2018.

[2] R. Carter, J. Mazurier, L. Pirro, J-U. Sachse, P. Baars, J. Faul, C. Grass, G. Grasshoff, P. Javorka, T. Kammler, A. Preusse, S. Nielsen, T. Heller, J. Schmidt, H. Niebojewski, P-Y. Chou, E. Smith, E. Erben, C. Metze, C. Bao, Y. Andee, I. Aydin, S. Morvan, J. Bernard, E. Bourjot, T. Feudel, D. Harame, R. Nelluri, H.-J. Thees, L. M-Meskamp, J. Kluth, R. Mulfinger, M. Rashed, R. Taylor, C. Weintraub, J. Hoentschel, M. Vinet, J. Schaeffer, and B. Rice. 22nm fdsoi technology for emerging mobile, internet-of-things, and rf applications. In *2016 IEEE International Electron Devices Meeting (IEDM)*, pages 2.2.1–2.2.4, 2016.

[3] B. Kazemi Esfeh, V. Kilchytska, B. Parvais, N. Planes, M. Haond, D. Flandre, and J.-P. Raskin. Back-gate bias effect on fdsoi mosfet rf figures of merits and parasitic elements. In *2017 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*, pages 228–230, April 2017.

[4] S.N. Ong, L.H.K. Chan, K.W.J. Chew, C.K. Lim, W. L. Oo, A. Bellaouar, C. Zhang, W.H. Chow, T. Chen, R. Rassel, J.S. Wong, C.W.F. Wan, J. Kim, W.H. Seet, and D. Harame. 22nm fd-soi technology with back-biasing capability offers excellent performance for enabling efficient, ultra-low power analog and rf/millimeter-wave designs. In *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 323–326, 2019.

[5] Athanasios Gatzastras, Christian Volmer, and Ingmar Kallfass. A differential travelling-wave amplifier in a 22nm fd-soi cmos technology. In *2022 14th German Microwave Conference (GeMiC)*, pages 108–111, 2022.